EK-MXV1B-UG-001

MXV11-B Multi-Function Option Module

User Guide

Prepared by Educational Services
of
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1 GENERAL DESCRIPTION

1.1 GENERAL

The M7195 module, designated MXV11-B, is a dual-height, multi-function option module compatible with LSI-11, LSI-11/2 and LSI-11/23 processors. The module can operate on the 22-bit Q-bus (up to 316K words), the 18-bit Q-bus, and the 16-bit Q-bus. MXV11-B features include:

- Read/write memory capability (MOS RAM)
- 5 V battery backup for MOS RAMs
- Read only memory (ROM)
- ROM window map logic (page control register)
- Two asynchronous serial line ports (SLU0, SLU1)
- Multiple line time clock frequencies
- LED diagnostic display register.

NOTE: The page control register, line time clock register, and diagnostic display register are user options and can only be selected if the MXV11-B is strapped for console port and bootstrap mode. Also, the Halt or Boot functions may be optionally selected in this configuration.

The following paragraphs describe these features. Figure 1-1 is a simplified block diagram of the module.

1.2 READ/WRITE MEMORY

The MXV11-B read/write memory consists of 128K bytes of dynamic MOS RAM without parity. The MOS RAMs operate off the system's +5 V supply or from the +5 V battery backup via a jumper consisting of a 0 ohm resistor. On-board memory refresh is included and is transparent to the user.

The read/write memory is configured from 64K SIPs (single in-line package). Four SIPs provide 64K 16-bit words or 128K bytes. RAM starting addresses are from 0 to 252K words on 4K word boundaries. This memory does not respond to addresses in the I/O page.

1.3 MOS RAM BATTERY BACKUP

The MXV11-B provides battery backup for the MOS RAMs. The battery backup must be jumpered to be functional, and battery backup power must be supplied by the system. A green light emitting diode connects across the MOS RAM power supply and ground to show that power is on to the RAMs.

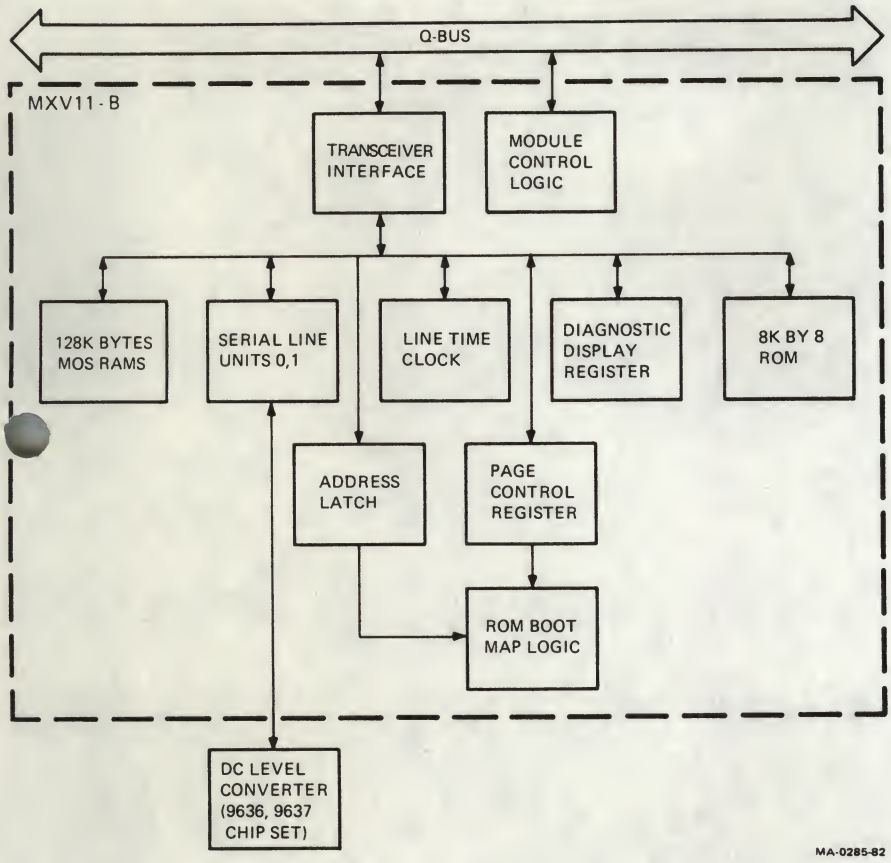


Figure 1-1 MXV11-B Simplified Block Diagram

READ ONLY MEMORY

Two 28-pin sockets on the +5 V read only memories (ROMs) contain bootstrap code, diagnostic code, or user routines. Wire-wrap posts allow the insertion of 2K by 8, 4K by 8, or 8K by 8 PROMs/ROMs in these sockets.

The PROM/ROM devices used may be ultra-violet Eraseable Programmable Read Only Memories, fusible link Programmable Read Only Memories, or masked Read Only Memories.

The 28-pin sockets can house user PROMs or the MXV11-B2 ROM set. If user PROMs are installed and are located in the user area (00000 through 077776 octal), the PROMs may only be directly addressed. If the user PROMs are located in the boot area, 773000_8, 765000_8 (18-bit address) they may be directly or indirectly addressed by a window mapping technique. (Refer to Paragraphs 1.4.1 and 1.4.2.)

If the MXV11-B2 ROM set is installed in the sockets, it can only reside in the boot area and may only be addressed by the window mapping technique.

Any size PROM (2K by 8, 4K by 8, or 8K by 8) can be addressed directly or indirectly via window mapping. One exception to this is the 2K by 8 UV (ultra violet) PROM which may be addressed only through direct addressing.

NOTE: To prevent wraparound, the PROM 1 and PROM 2 jumpers must be set to the correct PROM size.

1.4.1 Direct Addressing Mode

In direct addressing, ROM will reside in main memory, with starting addresses on any 4K word boundaries under 16K words (000000–777776 if 18-bit addressing is used). If that word bank is selected, only the space containing ROM is enabled, preventing "wraparound." Any read request made to ROM, where no ROM exists, results in no response from the module.

NOTE: All addresses specified in this manual are 18-bit.

Direct addressing can be used to access ROM in the I/O page when the ROM is used for bootstrapping. The bootstrap area consists of a 256 word block in the address range from 773000 to 773776. If an access is made to the ROM outside the bootstrap area, there is no response unless it is the address of an actual device in the system.

1.4.2 ROM Window Map

The ROM in the MXV11-B uses two windows in the I/O page. Each window points to 32 256-word blocks in ROM. This method of pointing prevents the whole I/O page from containing ROM code. Through this technique, any 256 word block of ROM can be transferred to the appropriate window area in the I/O page (Figure 1-2).

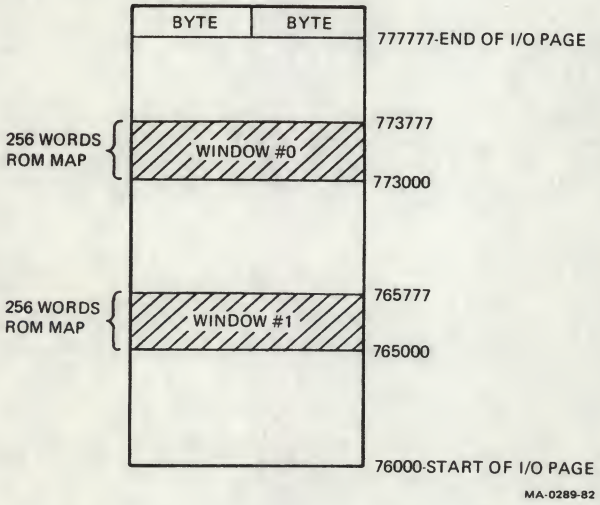


Figure 1-2 ROM Window Map Addresses (18 Bit Q-bus)

The ROM window addresses in Figure 1-2 are the addresses used by the 18-bit Q-bus. If the 16- or 22-bit Q-bus is used, the addresses are shown in Table 1-1. The window map is used when the MXV11-B is configured for bootstrap mode.

A page control register (PCR) in the MXV11-B, is used for the mapping feature. The PCR is a read/write register which supports DATIOB and DATOB operations. It resides at location 177520 in the I/O page and is two bytes in length.

The PCR which holds the window address fields points to one of the 256 word blocks to be accessed. The CPU reads the ROM via one of the two ROM window maps.

Each of these window maps (bootstrap areas) is pointed to by a five-bit address in the PCR. PCR format and bit assignments are shown in Figure 1-3. Bits 0 through 4 point to 1 of 32 256-word blocks in ROM (8K word space). The 256-word block pointed to by bits 0 through 4 is read through bootstrap address 773000_8. Bits 8 through 12 point to 1 of 32 256-word blocks in ROM. The 256-word block pointed to by bits 8 through 12 is read through bootstrap address 765000_8.

Table 1-1 ROM Window Addresses for 16-, 18-, and 22-bit Q-bus

Q-bus	Window 1 Start Addr (octal)	End Addr (octal)	Window 0 Start Addr (octal)	End Addr (octal)
16-bit	165000	165777	173000	173377
18-bit	765000	765777	773000	773377
22-bit	17765000	17765777	17773000	17773377

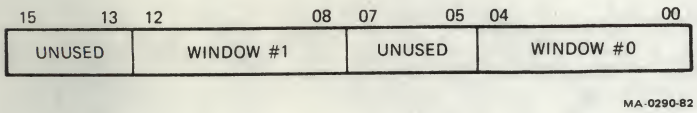


Figure 1-3 Page Control Register

1.5 SERIAL LINE UNITS

Data between the CPU and a peripheral device is serialized by an asynchronous serial line unit. The MXV11-B uses two of these lines, SLU 0 and SLU 1.

Each SLU contains a DLART which is a Universal Asynchronous Receiver/ Transmitter (UART) that has been modified by Digital Equipment Corporation. SLU 1 can be used as a console terminal port but SLU 0 cannot.

The serial line interfaces are configured so that SLU 0 is electrically closer than SLU 1 and therefore, has the higher interrupt priority.

The MXV11-B module also configures the SLUs so that SLU 1 tracks SLU 0. That is, SLU 1 is assigned to the next higher starting address over SLU 0. This is also true for the vector address assignments. An exception to this is when SLU 1 is assigned as the console port.

If SLU 1 is selected for console, the Halt and Boot options are normally enabled. These functions may be enabled under other conditions also. Either function is invoked when SLU 1 detects a break character. If the Halt option is selected, a break character halts program execution and the processor enters console ODT microcode. If the Boot option is selected, a break character initializes the system, then restarts the processor with the selected power up mode.

The baud rates for each serial line can be software programmable or can be strapped to 300, 1200, 9600, or 38,400.

The SLUs transmit and receive EIA-423 or RS 232 signal levels at 300, 1200, 9600, or 38,400 baud. A 20 mA active or passive current loop operation may be obtained with the DLV11-KA EIA to 20 mA converter option. The MXV11-B does not support the reader run portion of the DLV11-KA and does not contain modem control lines.

Break generation and error indicator bits the DLARTs provide overrun parity and framing errors. These errors can be read via the status registers. No parity bit or external baud rate clock logic is provided.

1.6 LINE TIME CLOCK

The line time clock (LTC) is a one-bit register (bit 06). When bit 06 is set, the clamp is removed from BEVENT thereby enabling the LTC. The address of the LTC is 777546. The LTC is derived from a 20 MHz crystal oscillator on the MXV11-B board. The crystal oscillator is also used for memory refresh.

NOTE: If a customer uses the LTC feature of the MXV11-B module, the module and the processor should be mounted in the same backplane.

A frequency divider connected to the oscillator provides a frequency of 617.4 KHz which is applied to the DLARTs of SLU1 and SLU0. The SLU1 DLART provides selectable line time clock frequencies of 50, 60, or 800 Hz. The desired frequency is selected by wire-wrapping the frequency to a common wire-wrap

post. The LTC can be enabled or disabled from driving the BEVENT line on the Q-bus by appropriate wire-wrap. The BEVENT line is used by the system for the real time clock (50 Hz, 60 Hz, or 800 Hz). The MXV11-B also provides a BEVENT clamp which holds BEVENT low at power-up to aid system diagnostics.

CAUTION: There should be only one source driver on the BEVENT line in any system. In most systems, the system power supply supplies the BEVENT signal. This source must be disabled if the MXV11-B is used to drive the line clock.

1.7 LED DIAGNOSTIC DISPLAY REGISTER

The MXV11-B contains a four-bit LED diagnostic display register (DDR) used for system diagnostics. The register is write-only but generates a reply on DATIO and DATIOB accesses. The DDR resides at location 777524 on the I/O page, and is enabled when the MXV11-B has its boot and console functions enabled.

1.8 MXV11-B2 BOOTSTRAP/DIAGNOSTIC ROM OPTION

The MXV11-B2 bootstrap/diagnostic ROM is a plug-in option for the MXV11-B. It performs bootstrap loading of programs (operating systems, for example) from mass storage devices and also performs diagnostic tests on the memory during power-up or when manually invoked. To install this option and configure the module and system it will be used in, refer to Chapter 3.

The bootstrap function is automatic on power-up if the CPU is configured for this feature. But an operator can intervene with a console terminal and boot devices at nonstandard I/O page addresses, select a secondary system device, or invoke a diagnostic utility.

Turnkey operation can be supported so that operator intervention is not needed to start the bootstrap function.

Some of the MXV11-B2 ROM features are listed below:

- Special standalone RT-11 volumes can be loaded and run.
- A system can be configured to down-line load via a DECnet link without operator intervention.
- All system devices currently available on the Q-bus are supported.
- Full 22-bit mapping support is included.

To use this option properly refer to the separate MXV11-B2 ROM Set User Guide (EK-MXVB2-UG) supplied with it.

NOTE: In order to use this ROM's examine/deposit command, the MXV11-B module must be contained in a 22-bit Q-bus system and must be configured to large systems (J37 jumpered to J36).

1.9 SPECIFICATIONS

The following paragraphs describe the physical, electrical, and environmental specifications for the MXV11-B module. The module is designed to the Q-bus specification.

1.9.1 Physical Specifications

Module:	Double height
Height:	5.187 inches
Width:	0.5 inch single layer
Length:	8.94 inches (bottom of fingers to top of handle extended)
Weight:	7.5 oz

1.9.2 Environmental Specifications

Temperature

Storage Temperature Range: –40° C to 66° C

Before using a module with a temperature beyond the operating range, bring the module to an environment within the operating range and then allow it to stabilize for a reasonable length of time (five or more minutes, depending on air circulation).

Operating Temperature Range: 5° C to 60° C

Derate the maximum operating temperature by 1.8° C for each 1000 meters of altitude above sea level.

Relative Humidity

Storage: 10% to 90%, noncondensing

Operating: 10% to 90%, noncondensing

Altitude

Storage: The module will not be mechanically or electrically damaged at altitudes up to 9 km.

Operating: Up to 3 km.

Airflow, Operating, Sea Level – Provide adequate airflow to limit the outlet temperature rise across the module to 5° C when the inlet temperature is 60° C. For operation below 55° C, provide airflow to limit the inlet to outlet temperature rise across the module to 10° C.

1.9.3 Random Access Memory Specification

Address Selection – RAM may be positioned on any 4K word boundary in the 0 to 252K word memory area. If bank select seven (BBS7) or bus refresh (BREF) is asserted, the memory will not respond.

1.9.4 Electrical Specifications

Power Requirements – The following voltages are used by this module.

Voltage	Tolerance	Pins
+5 V	±5%	AA2, BA2, BV1
+12 V	±5%	AD2, BD2
+5 VB	±5%	AV1

Power dissipated in each power supply configuration is as follows.

No battery backup

+5 V

Typ	17.25 W
Max	24.57 W

+12 V

Typ	0.67 W
Max	0.71 W

Battery backup configuration

+5 V

Typ	12.90 W
Max	15.95 W

+5 VB

Typ	4.35 W
Max	8.60 W

+12 V

Typ	0.67 W
Max	0.71 W

Data retention mode

VCC = 0 V, +12 V supply = 0

+5 VB

Typ	4.35 W
Max	5.54 W

FUNCTIONAL DESCRIPTION 2

2.1 GENERAL

This chapter describes the following functional areas of the MXV11-B.

ROM addressing (direct mode and page mode)
RAM memory
Line time clock
Crystal oscillator
Serial line units

The registers and bit formats are described in this chapter and are summarized in Appendix A.

2.2 PROM ADDRESSING

The PROM memory in the MXV11-B can be directly addressed (direct mode) via the Q-bus or indirectly addressed (page mode) via the two windows in the I/O page. Each window can specify 1 of 32 blocks (256 words per block). In direct mode or page mode, bits 14–15 (16-bit bus), 14–17 (18-bit bus) or 14–21 (22-bit bus), are used for address selection and are not used by the PROM.

2.2.1 Direct Addressing

Bits 9–13 (BDAL 9–BDAL 13) of the Q-bus are applied to the PROMs via tri-state drivers, bits 1–8 (BDAL 1–BDAL 8) are applied directly to the PROMs and bit 0 (BDAL 0) serves as a byte pointer. Figure 2-1 is a simplified block diagram showing how direct addressing and page addressing are implemented.

To directly address the PROMs you must leave the PG L/DIR H jumper disconnected. This turns the tri-state drivers on and address bits 9–13 are directly applied to the PROMs. As previously mentioned, bits 1–8 are wired directly to the PROMs.

When the page control register (PCR) is initialized both windows of this register point to the first location in window 0 which is 773000. This is the PCR default and allows all PROMs (whether 2K by 8, 4K by 8, or 8K by 8) to point to the same location. The PCR is primarily used in I/O page address mapping and is described in more detail in the next paragraph.

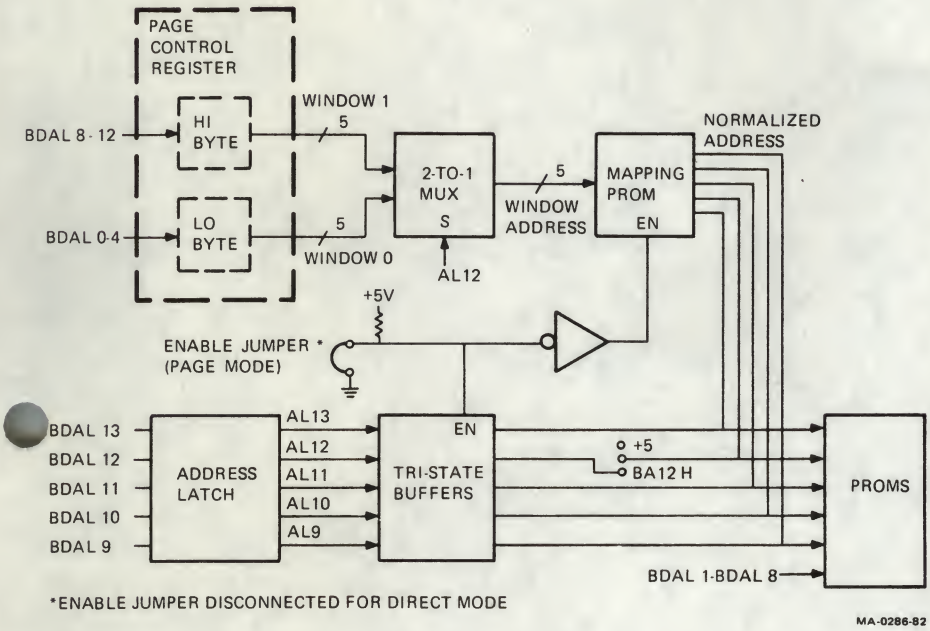


Figure 2-1 Direct and Page Addressing Block Diagram

2.2.2 I/O Page Addressing

To use page addressing you must connect the PG L/DIR H to GND jumper (J17 to J16), and BOOT L/PROM H to GND jumper (J44 to J45). Also, the boot ROM used must reside on the MXV11-B module. Then specify 1 of 32 256-word blocks of boot address space. The address space is selected by the read/write page control register (PCR). The PCR holds two window address fields, designated window 0 (773000–773776) and window 1 (765000–765776).

The CPU reads the 256 word ROM through one of two windows in the I/O page. The windows are pointed to by a 5-bit address field in the PCR. Bits 8–12 of the PCR point to window 1 and bits 0–4 point to window 0. The address of the PCR is 777520.

Figure 2-2 shows an example of how the page mode addressing is used. The window 0 field of the PCR is set to 30. As a result, the 256-word block addressed as 30 is read into the window 0 field (773000–773777) of the I/O page.

The window 1 field of the PCR is set to 2. The 256-word block addressed as 2 is read into the window 1 field (765000–765777) the I/O page.

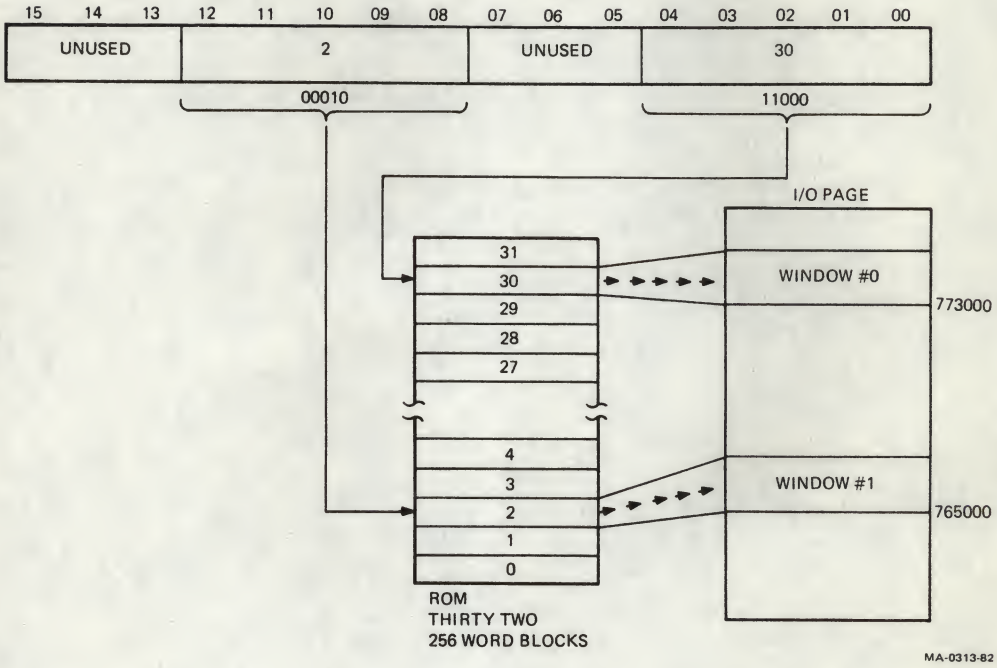


Figure 2-2 Page Mode Addressing

The window 1 and window 0 address are applied to a 2-to-1 multiplexer which multiplexes the window 1 or window 0 address to the output depending on the state of address line 12 (BDAL 12). The 5-bit window address is applied to a mapping PROM which is enabled by the PG L/DIR H jumper (J17) being connected. This jumper turns off the tri-state drivers causing the output of the tri-state lines to be high impedance. Note that the tri-state drivers are turned on during direct mode addressing and are turned off during window mapping.

The mapping PROM normalizes the window address – the normalized address is derived from the true address via a mapping matrix. Table 2-1 shows the true addresses (window block) and the corresponding normalized (ROM) addresses.

The 5-bit normalized address is connected to the tri-state output lines which are now high impedance. As a result, the normalized address is applied to the PROMs.

The 32 blocks of memory may not be contiguous. The mapping function takes care of this and its operation is transparent to the user.

Table 2-1 ROM Window Map

Window Field	Normalized 0 ROM Address	
0	00000	
1	01000	
2	02000	
3	03000	
4	04000	
5	05000	
6	06000	
7	07000	Maximum address for 2K by 8 PROM
10	10000	
11	11000	
12	12000	
13	13000	
14	14000	
15	15000	
16	16000	
17	17000	Maximum address for 4K by 8 PROM
20	20000	
21	21000	
22	22000	
23	23000	
24	24000	
25	25000	
26	26000	
27	27000	
30	30000	
31	31000	
32	32000	
33	33000	
34	34000	
35	35000	
36	36000	
37	37000	Maximum address for 8K by 8 PROM

2.3 RAM MEMORY FUNCTIONAL DESCRIPTION

Figure 2-3 shows a simplified block diagram of the RAM memory. The memory consists of 64K by 4 Single In-line Packages (SIPs). The following paragraphs describe read/write memory access, refresh access, and the arbitration logic for memory access.

2.3.1 Read/Write Access

The address from the Q-bus is saved in an address latch through a set of Q-bus transceiver interfaces. The address is then separated into high and low bytes by a 16-to-8 line multiplexer. These bytes are then applied to the RAM address lines via a second multiplexer which selects between the bus address or a refresh address. The second multiplexer is formed by the tri-state outputs of the refresh counter and the 16-to-8 multiplexer. Refresh has priority over RAM read/write request and peripheral I/O (PIO) requests.

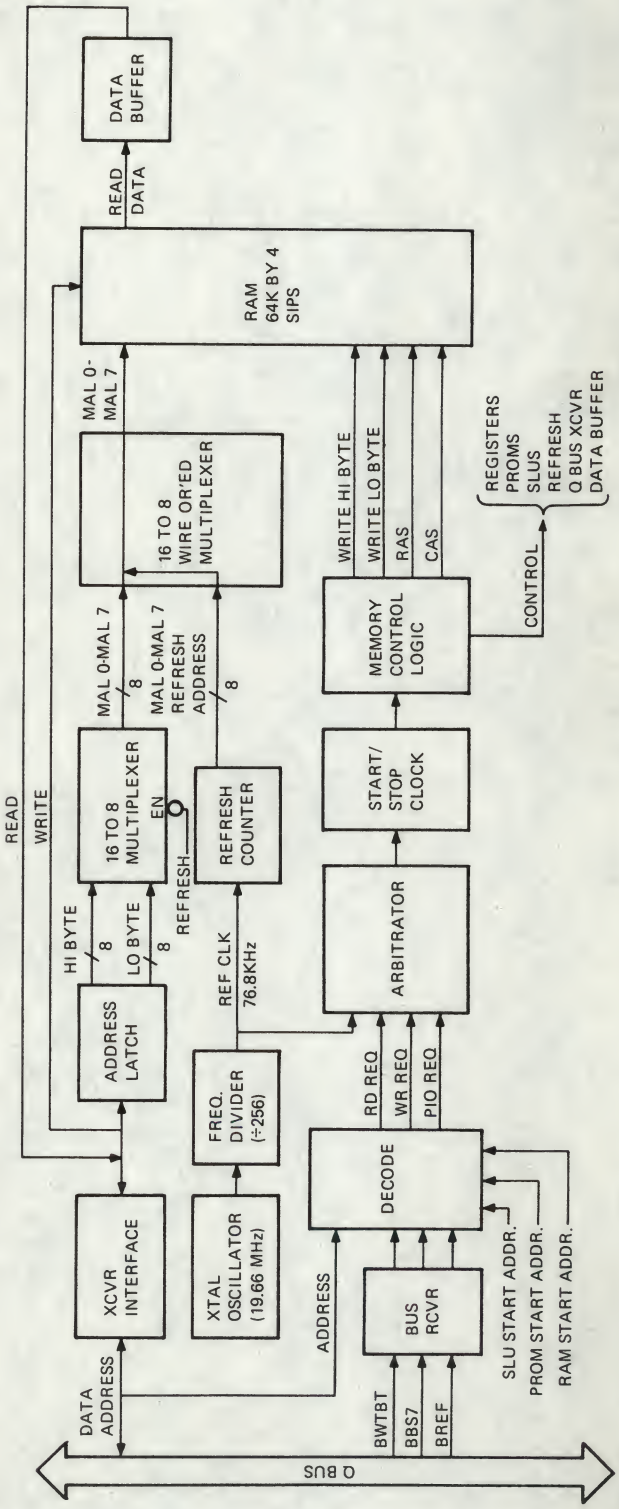


Figure 2-3 RAM Memory Functional Block Diagram

However, if a read or write memory cycle is in progress, that cycle completes before a refresh cycle starts. On a read cycle, the read data from memory is applied to a data buffer and then to the transceiver interface for transfer to the Q-bus. On a write cycle, the data from the Q-bus is applied to the transceiver interface and then directly to the memory.

2.3.2 Refresh Access

The RAM memory is refreshed at a 76.8 KHz rate. This rate is obtained from a 19.660 MHz crystal oscillator which has been applied to a frequency divider. The divider divides the frequency by 256 to yield 76.8 KHz. This frequency is applied to a refresh counter which refreshes each row of the MOS RAMs at the 76.8 KHz rate.

2.3.3 Arbitration Logic

Bits 13–15 of the 16-bit Q-bus address are applied to the decode logic. For the 18-bit Q-bus, bits 13–17 are applied to the decode logic, and for the 22-bit Q-bus bits 13–21 are applied to the decode logic. This address is the address the CPU wants to access.

The SLU start address, the PROM start address, and the RAM start address are selected by wire-wrap pins on the MXV11-B module. These addresses are also applied to the decode logic.

Finally, BWTBT (Bus Write Byte), BBS7 (Bus Bank Select 7), and BREF (Bus Refresh) are applied to the decoder via bus receivers. The decode logic decodes all these inputs and outputs a RD REQ, WR REQ, or PIO REQ.

If the BBS7 signal is asserted at the input to the decode logic, memory will not respond and the system can only access the I/O page. If the BREF signal is asserted, memory will not respond. If the BWTBT signal is asserted, it indicates a DATO(B) operation will occur. If BWTBT is negated, a DATI or DATI(B) operation will occur. In order for the DATO or DATI operation to occur, BREF must be negated.

If the CPU is doing a write operation to memory, BWTBT is asserted and the decode logic asserts WR REQ. If the write operation is to the I/O page, BBS7 is also asserted. Conversely, if the CPU is doing a read operation, BWTBT is negated, and the decode logic outputs RD REQ.

PIO REQ is asserted when access is made to a boot ROM, SLU, or I/O page register (LTC, PCR, or DDR).

The RD REQ, WR REQ, and PIO REQ signals are mutually exclusive in that only one of the signals can be asserted at any given time. These signals, along with the REF REQ signal are applied to the arbitration logic which arbitrates between REF REQ and one of the other requests (RD REQ, WR REQ, or PIO REQ). The first request is the one that is serviced first. But, when a REF REQ *and* RD REQ, WR REQ, *or* PIO REQ occur almost simultaneously, the arbitration logic decides which request gets serviced first.

When this decision is made, the output of the arbitration logic starts the clock to initiate the memory access via the memory control logic. If the memory access is a write word, the WRITE HI BYTE, WRITE LO BYTE, RAS and CAS signals are all asserted by the memory control logic. If the memory access is a write byte, the appropriate byte signal (WRITE HIGH BYTE or WRITE LO BYTE), and the RAS and CAS signals are asserted. Data from the Q-bus is fed to the RAM via the transceiver interface.

If the memory access is a read request, the WRITE HI BYTE and WRITE LO BYTE signals are negated and the RAS amd CAS signals are asserted. Data from memory is applied to a data buffer, the transceiver interface, and then to the CPU via the Q-bus.

The memory control logic also provides control signals for the MXV11-B registers, PROMs, serial line units, refresh circuit, transceivers, and the data buffer.

2.4 CRYSTAL OSCILLATOR

The crystal oscillator (Figure 2-4) in the MXV11-B oscillates at 19.66 MHz. The oscillator's output is applied to an 8-bit frequency divider. The divider divides the oscillator frequency for the various system functions described below.

The DCLK signal is derived from the oscillator and clocks the DLARTs. The DCLK signal is 614.4 KHz (19.66 MHz divided by 32). There is a DLART for each SLU. The line time clock for the MXV11-B is obtained from one of three selectable frequency outputs of the DLART. The DLART has outputs of 800 Hz, 60 Hz, and 50 Hz. One of these frequencies is chosen by wire-wrapping the appropriate pins.

The PCLK signal of 307.2 KHz (19.66 MHz divided by 64) clocks the −12 V charge pump circuit. The REF CLK of 76.8 KHz (19.66 MHz divided by 256) clocks the refresh counter. Each row of RAM memory chips is refreshed at the 76.8 KHz rate.

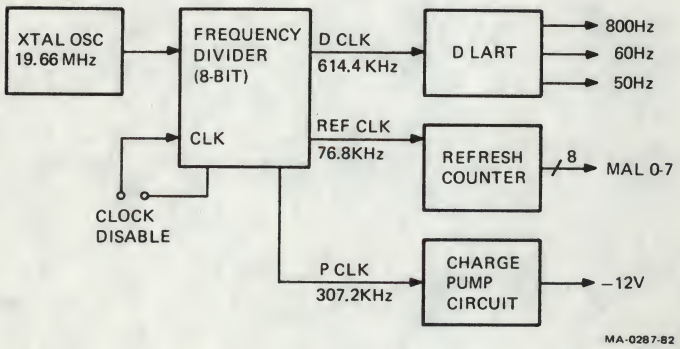


Figure 2-4 XTAL Oscillator Block Diagram

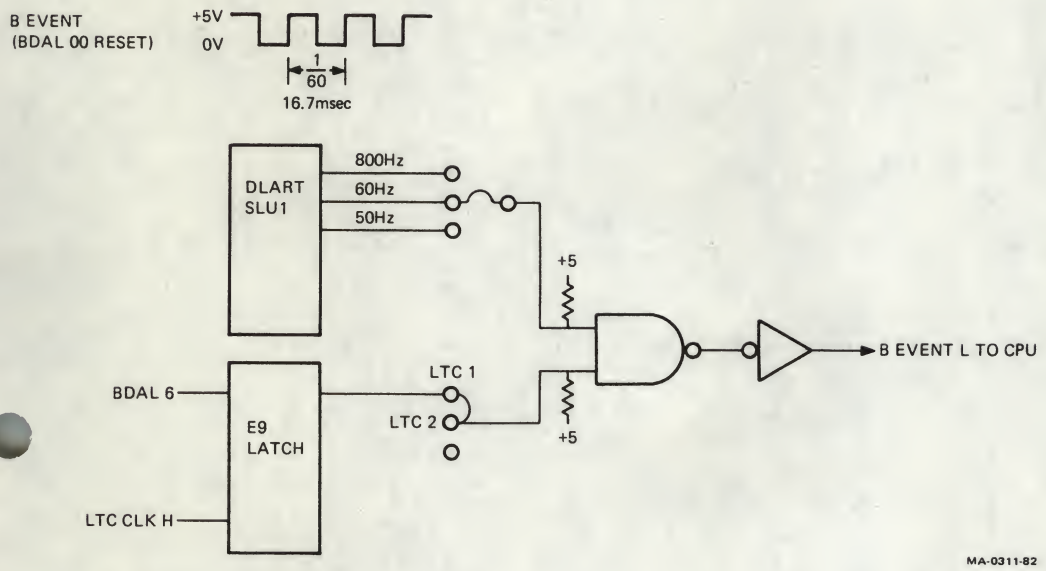


Figure 2-5 Line Time Clock Diagram

2.5 LINE TIME CLOCK

Figure 2-5 is a simplified block diagram of the line time clock logic. The DLART associated with SLU 1 has selectable frequency outputs of 800 Hz, 60 Hz, and 50 Hz. To use one of these frequencies as the line time clock, the appropriate post must be wire-wrapped. Figure 2-5 shows the 60 Hz frequency selected. In addition, bit 6 of the LTC latch must be set and the LTC 1 to LTC 2 jumper must be connected. This allows BEVENT L to be driven at a 60 Hz rate by the MXV11-B. In most Digital systems, the power supply drives BEVENT.

CAUTION: There can only be one source of BEVENT in a system.

2.6 DIAGNOSTIC DISPLAY REGISTER

The diagnostic display register (DDR) resides at location 777524 in the I/O page. It is a write-only register but generates a reply on DATIOB and DATOB accesses. DDR is only enabled when the MXV11-B has its Boot and Console functions enabled.

Only bits 0–3 of the 16-bit word are used. These bits correspond to four red LEDs on the board (bit 3 is the MSB and bit 0 is the LSB). Figure 2-6 shows five LEDs – the four red LEDs comprise the DDR and the green LED indicates power-on.

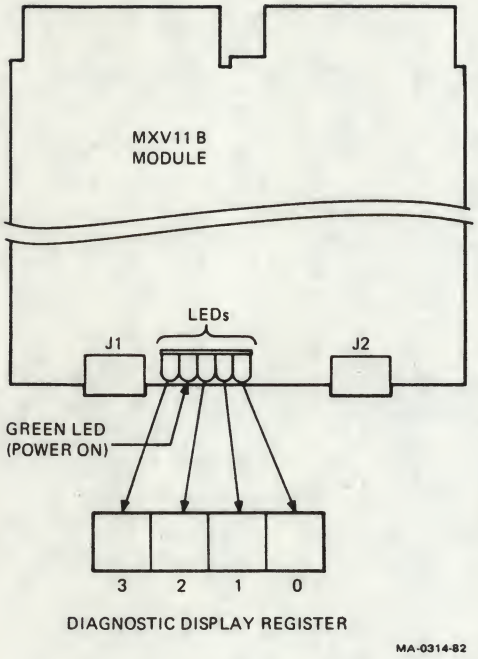


Figure 2-6 MXV11-B Diagnostic Register (LEDs)

2.7 SERIAL LINE UNITS

Data between the peripheral and the DLART in the SLU is transmitted serially. Data between the DLART and the CPU is transmitted in parallel and consists of characters containing eight data bits without parity. A start bit and a stop bit is associated with each character. A standard EIA interface connects the DLART to the peripheral device. If a 20 mA loop is required, the DLV11-KA option is used.

The following paragraphs describe address selection, interrupt vector selection, baud rate selection, and register bit assignments of the serial line units.

2.7.1 Address Selection

Serial line unit 0 may be assigned to any one of eight starting locations in the I/O address space range from 776500 to 776570. Serial line unit 1 is automatically assigned by the MXV11-B to the next higher starting address over SLU 0. The I/O address assignment for SLU 1 is from 776510 and 776600.

When SLU 1 is assigned the console port, it assumes address 777560. Default addresses are 776500 for SLU 0 and console port for SLU 1.

2.7.2 Interrupt Vector Selection

Vector address selection covers the vector address space from 010–376.

NOTE: Be careful – some addresses are reserved.

Bits 3–7 of the vector address can be programmed (via wire-wrap) to select independent vector addresses for each of the serial line units. Bits 0, 1, and 8 are always 0 for the MXV11-B (Figure 2-7).

The vector assignment for SLU 1 is the next higher vector location over SLU 0. The exception is if SLU 1 is selected as the console port. In this case, serial line unit 1 has a vector address of 060 for the transmitter and 064 for the receiver.

Each of the DLART transmit and receive registers track each other. Bit 2 of the vector address automatically selects a zero for the receiver and a one for the transmitter of each serial line interface.

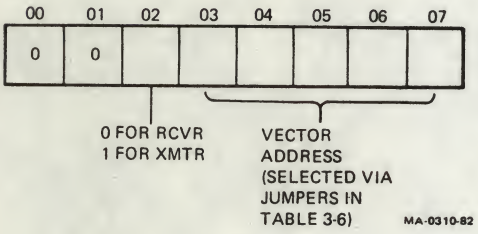


Figure 2-7 SLU Vector Address Bit Format

2.7.3 SLU Register Addressing

The MXV11-B has four registers associated with each of the two SLUs. The registers for SLU 0 are:

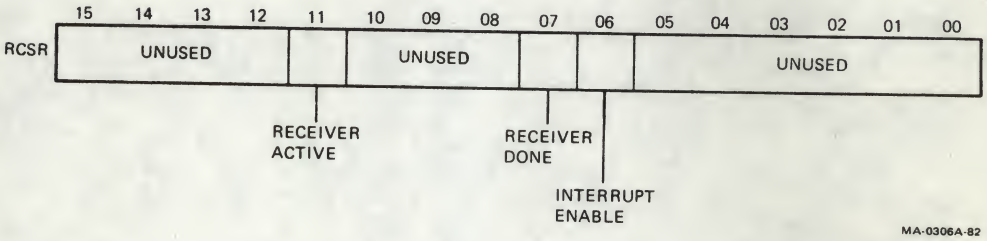
Receiver control/status register	(RCSR 0) – Table 2-2
Receiver data buffer	(RBUF 0) – Table 2-3
Transmitter control/status register	(XCSR 0) – Table 2-4
Transmitter data buffer	(XBUF 0) – Table 2-5.

The registers for SLU 1 are:

Receiver control/status register	(RCSR 1) – Table 2-2
Receiver data buffer	(RBUF 1) – Table 2-3
Transmitter control/status register	(XCSR 1) – Table 2-4
Transmitter data buffer	(XBUF 1) – Table 2-5.

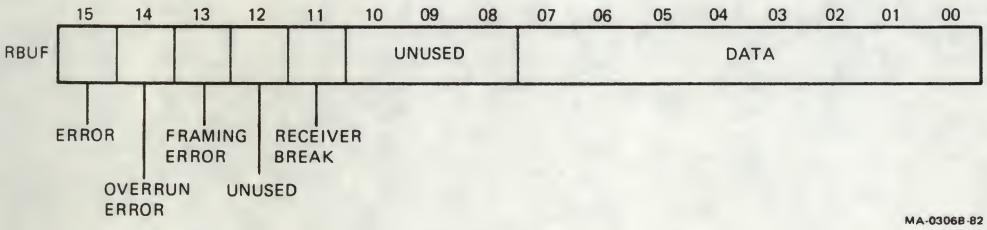
Both SLUs have the same bit assignments and are located in the I/O page. BBS7, when asserted, specifies the I/O page and bits A3–A12 specify the peripheral device in the I/O page. SLU 0 can be assigned one of eight addresses (Table 3-5). SLU 1 can be assigned one of eight addresses and may be assigned as the console port (777560).

Table 2-2 Receiver Status Register Bit Assignments (RCSR)



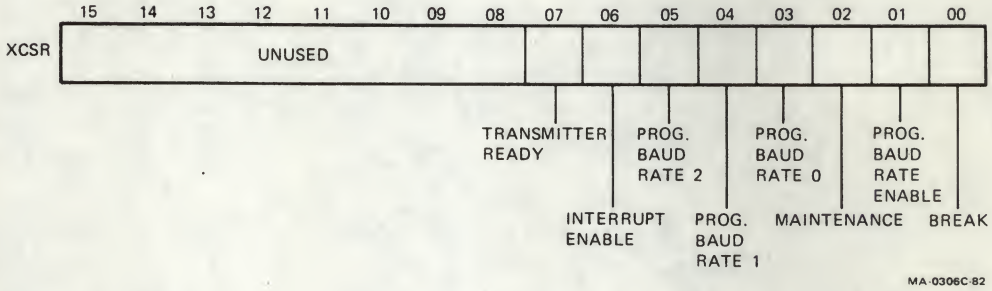
Bit		Description
15–12		Unused
11	RA Receiver active read only	A logic one indicates that the receiver is active. Set at the center of the start bit of the input serial data. Cleared at the expected center of the stop bit at the end of the time prior to the leading edge of RCV DONE. Also cleared by power up sequence.
10–8		Unused
7	RD Receiver done read only	A logic one indicates that the serial interface has received a character. If enabled by bit 6, receiver done requests an interrupt. Receiver done is cleared by reading the receiver data register or by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables receiver interrupts; a zero disables interrupts. Cleared by Initialization.
5–0		Unused

Table 2-3 Receiver Data Buffer Bit Assignments (RBUF)



Bit		Description
15	ER Error read only	A logic one indicates that bit 13 and/or bit 14 is a one. Cleared when the bit is read or cleared by power-up sequence.
14	OE Overrun error read only	A logic one indicates a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read or by power-up sequence.
13	FE Framing error read only	A logic one indicates that a start bit was detected but there was no corresponding stop bit. A framing error is generated when a break is received. Cleared when read or by power-up sequence.
12		Unused
11	RB Receiver break read only	This bit is set when serial-in (SI) signal goes from a mark to a space and stays in the space condition for 11 bit times after serial reception starts. This bit is cleared when the SI signal returns to the Mark condition, or by power-up sequence.
10–8		Unused
7–0	Data read only	These eight bits hold the most recent byte received. When a new byte is transferred to the data buffer, the RCV DONE in the RCSR is set. Bit 0 is the LSB and bit 7 is the MSB. Cleared by power-up sequence.

Table 2-4 Transmitter Status Register Bit Assignments (XCSR)



Bit		Description
15–8		Unused
7	TR Transmitter ready read only	A logic one indicates the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready requests an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables transmitter interrupts. A logic zero disables interrupts. Cleared by initialization.
5–3	BR2-BR0* Programmable baud rate select read/write	When PBR-bit 1 in XCSR is set, these bits determine the baud rate (set by software if SOFT jumper connected to GND). If SOFT jumper is connected to OPEN, baud rate is obtained via wire-wrap. Bits BR2-BR0 are cleared by PBR Inhibit (SOFT EN) or by power-up sequence.
2	MAINT Maintenance read/write	This bit facilitates a maintenance self-test. When the bit is set, the transmitter serial output is connected to the receiver serial input and the external serial input is disconnected. This bit is cleared by initialization.

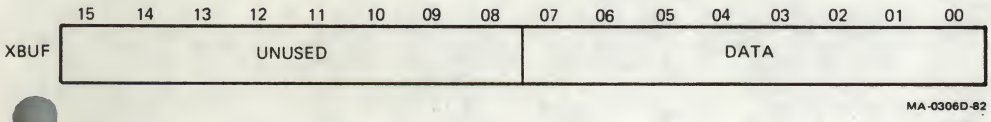
* Read only as a zero when PBRI (programmable baud rate inhibit) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper– J14–J15).

Table 2-4 Transmitter Status Register Bit Assignments (XCSR) (Cont)

Bit		Description
1	PBR* Programmable baud rate enable Read/write when software programmable baud rates enabled (SOFT to GND jumper); else read only as 0	This bit selects between internal and external baud rate selection. When set (enable), the baud rate is determined by the PBR2-0 bits in this register. When clear (inhibit), the baud rate is determined by the J1, J0 wire-wrap pins. This bit is cleared by power-up sequence or SOFT to OPEN Jumper connected (programmable baud rate inhibit (J14 to J15).
0	BK Break read/write	When this bit is set, it causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by bus initialization.

* Read only as a zero when PBRI (programmable baud rate inhibit) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper– J14–J15).

Table 2-5 Transmitter Data Buffer Bit Assignments (XBUF)



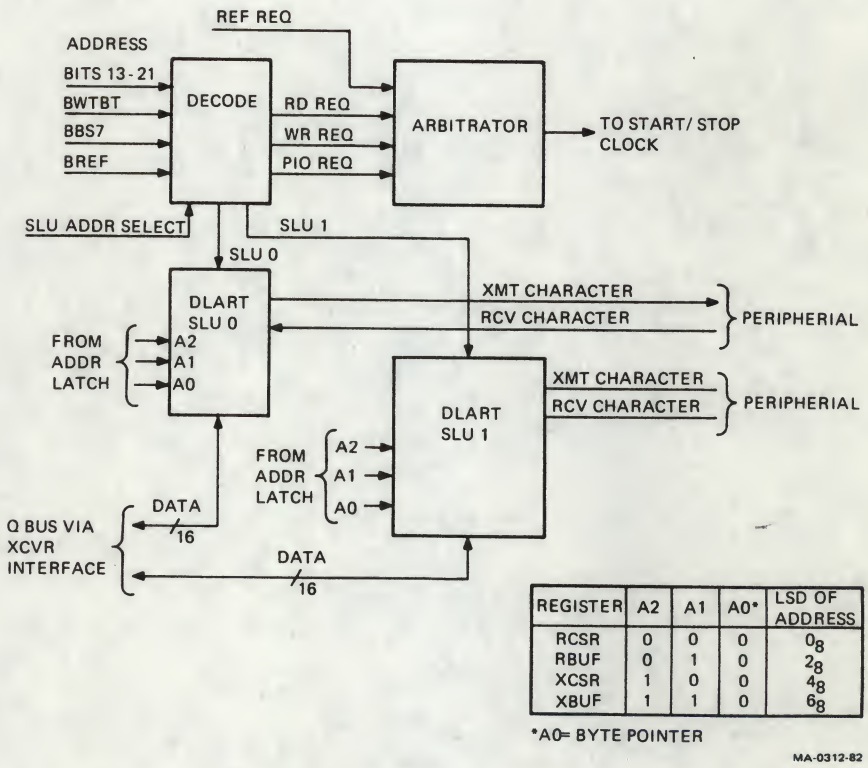
Bit		Description
15–8		Unused
7–0	XMIT DATA BUFFER read/write	Transmitter data buffer – this byte register holds a copy of the most recent byte written into it. When a byte is written into this register, the transmit ready (TR) bit in the XCSR register is cleared. This byte is copied into the transmitter serial output register whenever that register is empty and the bit is clear. The TR bit is set when a byte is copied from the transmitter data buffer into the serial output register. Reading the contents of this register causes no other effect. Cleared by power-up sequence.

The SLU registers for both SLUs are addressed via address lines A2, A1, and A0 from the address latch (Figure 2-8). The address latch and decoder are the same as shown in Figure 2-3. A2, A1, and A0 are applied to both SLUs. The SLU selected is determined by the chip select (CS) input to the DLART and is a function of the decode logic.

The chart in Figure 2-8 shows how A2, A1, and A0 select one of the four DLART registers by determining the least significant octal digit of the address.

NOTE: All bits in the SLU registers are reset by a power-down/power-up sequence which causes signals BDC OK H and BINIT L to go low and then go high.

These bits are also reset if the operator presses a restart switch contained in certain systems. There are certain bits (Interrupt Enable, Break, and Maint) in the SLU registers which may be cleared by bus initialization and by the power-up sequence (refer to Tables 2-2 through 2-5).



REGISTER	A2	A1	A0*	LSD OF ADDRESS
RCSR	0	0	0	0_8
RBUF	0	1	0	2_8
XCSR	1	0	0	4_8
XBUF	1	1	0	6_8

*A0= BYTE POINTER

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Figure 2-8 SLU Register Addressing

2.7.4 Baud Rate Selection

The baud rates are the same for transmit and receive functions of the same DLART. The baud rates can be set via strapping or by software programming.

Strapped Baud Rates – Each of the SLUs can be strapped to one of four baud rates (300, 1200, 9600, and 38.4K) when the SOFT EN to OPEN jumper is connected. This disables the software programmed baud rates in both SLUs.

Each SLU has a set of two wire-wrap posts strapped in various combinations to select the desired baud rate (Table 3-4).

Software Programmed Baud Rates – The software programmed baud rates are enabled if the SOFT EN wire-wrap post is strapped to GND (J14 to J13). Software then has to write the XCSR (Paragraph 2.7.3) of each DLART to set up the baud rates.

In order to enable software controlled baud rates, SOFT EN must be jumpered to GND (J14 to J13) and the programmable baud rate enable (PBRE) bit (bit 1 of XCSR) must be set. If this bit is not set, the strapped (hardware controlled) pins (Table 3-4) determine the baud rate. With PBRE set, the programmable baud rate bits (PBR 2, 1, and 0 in XCSR) select the baud rate in accordance with this chart.

PBR 2	1	0	PBRE	Octal Data	Baud Rate
0	0	0	1	002	300
0	0	1	1	012	600
0	1	0	1	022	1200
0	1	1	1	032	2400
1	0	0	1	042	4800
1	0	1	1	052	9600
1	1	0	1	062	19200
1	1	1	1	072	38400

At power up, if SOFT EN is connected to GND (J14 to J13), the software baud rates are enabled. PBR 2, 1, and 0 are reset to 0 which defaults to 300 baud. If the PBRE bit is set to 0, the DLARTs monitor the hardware selectable baud rates (jumpers J7–J11).

If the operator sets PBRE to 1, the DLART disregards the jumpers and uses the baud rates determined by PBR 2, 1, and 0. Those bits must be set to their proper baud rates.

If the SOFT EN jumper is not connected to GND at power up, the baud rate is determined by hardware selectable baud rate jumpers J7–J11.

2.8 CABLES

Table 2-6 lists part numbers, options, applications, and cabling lengths available for the MXV11-B module. Digital offers the BC20M-50 cable for MXV11-B to DLV11-J operation. Because longer cables usually require routing without connectors attached, the user should make cables for lengths greater than 15 meters (50 feet). Cable material must adhere to EIA RS-423 specifications. The connectors on the MXV11-B module are AMP-87272-8 (2 pin × 5 pin on 0.1 inch centers). These connectors can mate with a wide variety of low cost cables including 10-conductor flat cable. Note that a pin 1 baud rate clock is not used on this module.

Pin 10 carries +12 Vdc to supply power for the DLV11-KA option. Therefore, pins 1 and 10 should be unterminated if the DLV11-KA option is not used. Cable retention in the module is provided by locking clip contacts (AMP PN87124-1).

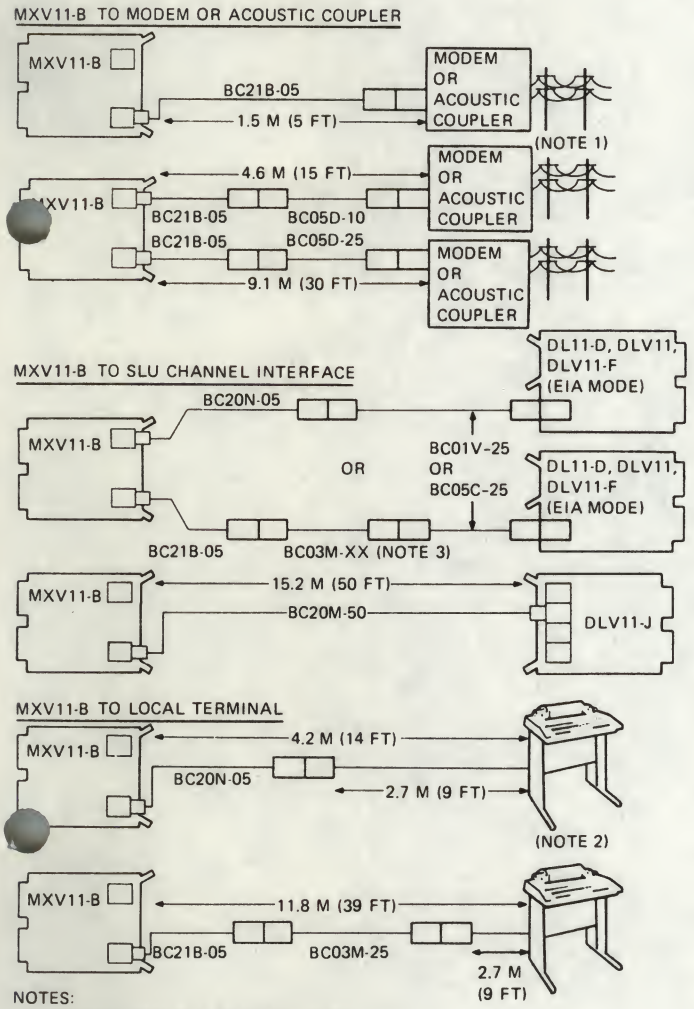
The locking clips hold the receptacle (AMP PN87133-5) in the module connector when the cable is pulled. To remove the cable from the connector, pull back the cable receptacle to disengage the locking clips.

Table 2-6 Definition of Cables

Cable	Application	Length
BC21B-05	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male)	1.5 m (5 ft)
BC20N-05	EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5 pin AMP female to RS-232C female)	1.5 m (5 ft)
BC20M-50	EIA RS-422 or RS-423 cable for high-speed transmission (19,200 baud) (2 × 5 pin AMP female to 2 × 5 AMP female)	15 m (50 ft)
BC05D-10	Extension cable used in conjunction with BC21B-05	3 m (10 ft)
BC05D-25	Extension cable used in conjunction with BC21B-05	7.6 m (25 ft)
BC03M-25	"Null modem" extension cable used in conjunction with BC21B-05	7.6 m (25 ft)

Note: "Strapped" logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

The MXV11-B may operate with several peripheral device cables and options for flexibility when configuring systems. Figures 2-9 and 2-10 show the variety of cables and options used with the MXV11B the primary application of each.

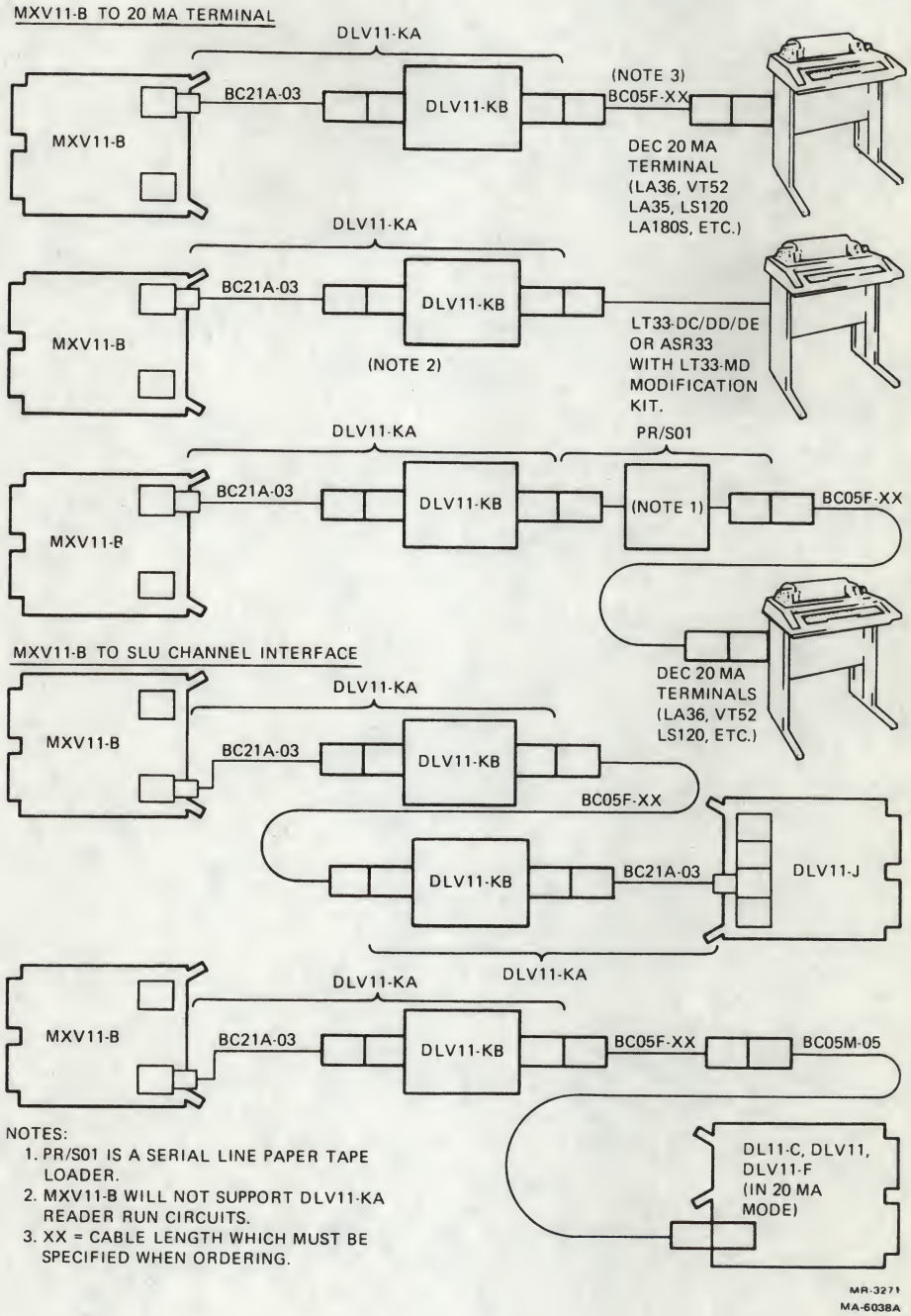


NOTES:

1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIS RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.
3. XX = CABLE LENGTH WHICH MUST BE SPECIFIED WHEN ORDERING.

MR 3270
MA-6037A

Figure 2-9 MXV11-B EIA Cable Configurations



NOTES:
1. PR/S01 IS A SERIAL LINE PAPER TAPE LOADER.
2. MXV11-B WILL NOT SUPPORT DLV11-KA READER RUN CIRCUITS.
3. XX = CABLE LENGTH WHICH MUST BE SPECIFIED WHEN ORDERING.

Figure 2-10 MXV11-B 20 mA Cable Configurations

When designing a cable for the MXV11-B, consider these several points:

1. To connect directly to a local EIA RS-232C terminal, you must use a null modem. To design the null modem into the cable, switch Received Data (pin 2) with Transmitted Data (pin 3) on the RS-232C male connector as shown (Figure 2-11).

2. The receivers on the MXV11-B have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, you must tie Receive Data (pin 7 on the 2 × 5 pin AMP connector) to signal ground (pins 2, 5, or 9) in order to maintain proper EIA levels (Figure 2-12).

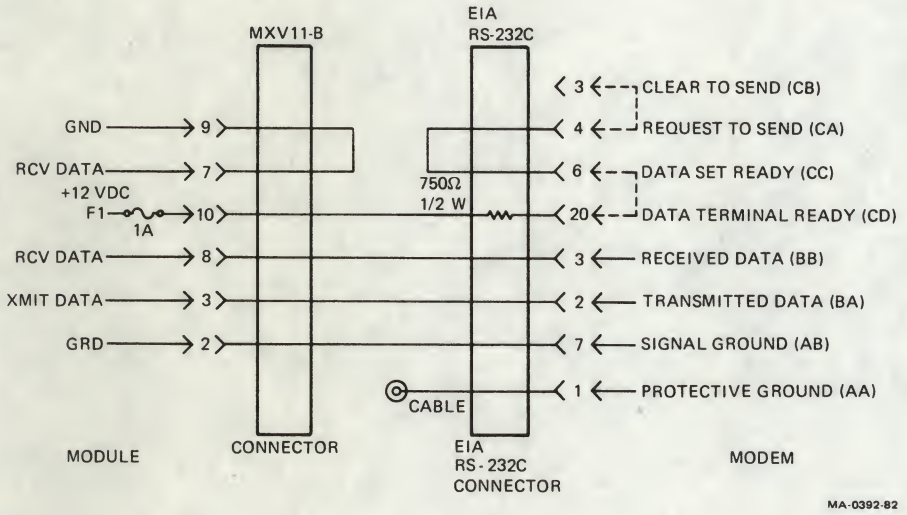


Figure 2-11 BC21B-05 Modem Cable

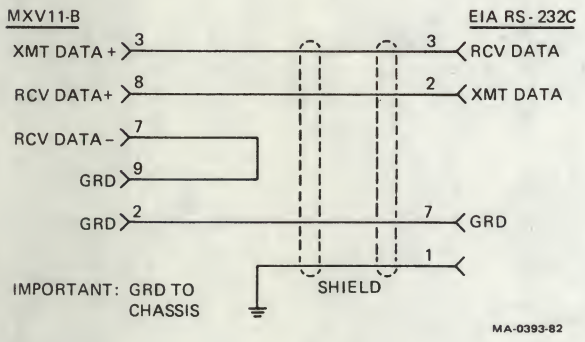


Figure 2-12 BC20N-05 Null Modem Cable

To mate to the 2 × 5 pin connector block, you need the following parts.

Cable receptacle (1)	AMP PN 87133-5 DEC PN 12-14268-02
Locking clip contacts (9)	AMP PN 87124-1 DEC PN 12-14267-00
Key pin (pin 6) (1)	AMP PN 87179-1 DEC PN 12-15418-00

2.8.1 Interface Connector Pins

Two 10-pin connectors (one for each serial line) are provided on the MXV11-B module. Connector pins and signal functions are described in Table 2-7 and shown in Figure 2-13.

Table 2-7 MXV11-B I/O Connector Pin Functions

Pin	Signal	Function
1	BRCLK	Baud rate clock. This output provides a clock signal at a frequency of 16 times the selected aud rate. This pin is used as an output from the MXV11-B and does not accept external clock inputs.
2	Ground	
3	XMIT	Transmitter output
4	Ground	
5	Ground	
6	NC	Key, pin not provided
7	RCV−	Receiver input most negative
8	RCV+	Receiver input most positive
9	Ground	
10	+12 V	Power for the DLV11-KA option

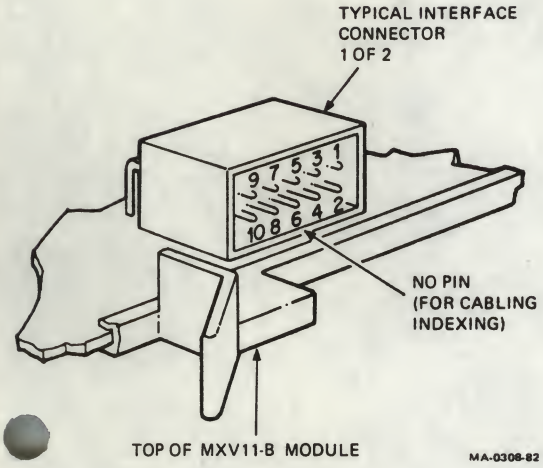


Figure 2-13 MXV11-B Connector Pins

2.8.2 Current Loop

The MXV11-B module can interface with 20 mA active or passive current loop devices when used with the DLV11-KA option. This option consists of a DLV11-KB (EIA-to-20 mA current loop converter) and a BC21A-03 interface cable. The MXV11-B cannot support the reader run portion of the DLV11-KA option. The DLV11-KA option is placed between the MXV11-B serial line output and the 20 mA current loop peripheral device. Figure 2-10 shows the cables and devices which may be used with the DLV11-KA option.

3 JUMPER CONFIGURATIONS

3.1 GENERAL

This chapter describes how the user can configure the MXV11-B module to function properly in his system. The jumpers used with this module are of two types – push-on connectors and wire-wrap. However, sometimes the user has to wire-wrap certain jumpers (for example, line time clock jumpers). The push-on connectors are associated with grouping of pins where one of the pins is open. These connectors allow two adjacent pins to be jumpered. If the jumper relating to a function is to remain disconnected, one pin of the push-on connector is placed on the pin associated with that function. The other pin of the push-on connector is placed on the open pin, which is not connected to ground, +5 V, or any logic function, and merely serves as a holder for the push-on connector. If a push-on connector is missing, a wire-wrap jumper may be substituted. When installing jumpers, arrange the wire runs so that no more than two wires are on each post and there is no level jumping between posts.

MXV11-B modules shipped from the factory have a 0 ohm resistor supplying the MOS RAMs with nonbattery backup power of +5 V; 8 push-on connectors; and no wire-wrap jumpers connected. Figure 3-1 shows the default configuration for the push-on connectors designated W3–W10. There are two 0 ohm resistors used for battery backup connections: W1 and W2. Only one of them may be inserted at a time. For nonbattery backup applications, W2 is inserted. Paragraph 3-2 summarizes these default conditions and the defaults for the wire-wrap jumpers.

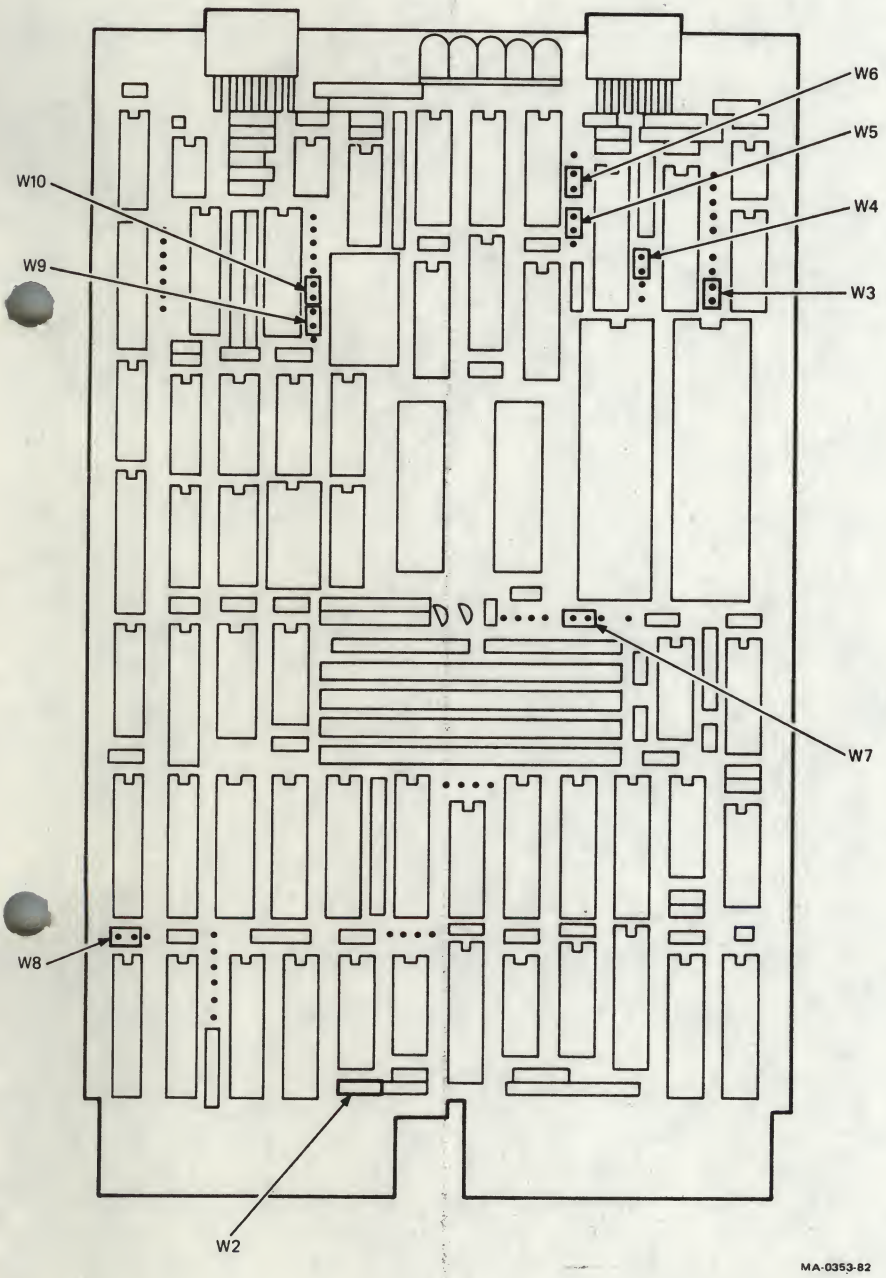


Figure 3-1 Default Configuration of Push-On Connectors

Before trying to configure the MXV11-B module, complete the following checklist. The checklist, jumper locations in Figure 3-2, the flow diagram in Figure 3-3, and the tables in this chapter should be used when configuring a system.

		User's Configuration	Shipped Configuration
1)	Do you wish to connect the system console to this MXV11-B? If no, disregard following questions marked with an *. If yes, the console must be connected to SLU #1.	_____	Yes
2)*	Do you wish system to halt on break from console?	_____	Yes
3)*	Do you wish system to reboot on break from console?	_____	No
4)	What is desired address/ vector for SLU 0?	_____/____	776500/300
5)	What is desired address/ vector for SLU 1?	_____/____	777560/60
6)*	Will this MXV11-B contain MXV11-B2 ROM?	_____	No
7)	Will this MXV11-B contain user ROM?	_____	No
	If yes, at what address?	_____	N/A
	*Are user ROMs to be addressed via page mode?	_____	N/A
	What is ROM size?	_____	N/A
	What is ROM type?	_____	N/A

		User's Configuration	Shipped Configuration
8)*	Do you want software control of line time clock ( )?	_____	No
9)	Does this system have "Q" or "Q22" bus?	_____	Q Bus
10)	Do you wish this module to be source of line time clock (BEVENTL)?	_____	No
11)	If yes, at what frequency (50, 60, or 800 Hz)?	_____	
12)	Do you wish software control of baud rate?	_____	No
13)	What hardware controlled baud rates are desired? SLU0/SLU1	_____	300/9600
14)	Is battery backup desired for RAM memory?	_____	No
15)	What is RAM starting address?	_____	000000

A series of tables in this chapter describe the jumpers on the module. An associated figure (Figure 3-2) shows the physical location of the jumpers with respect to the ICs on the module.

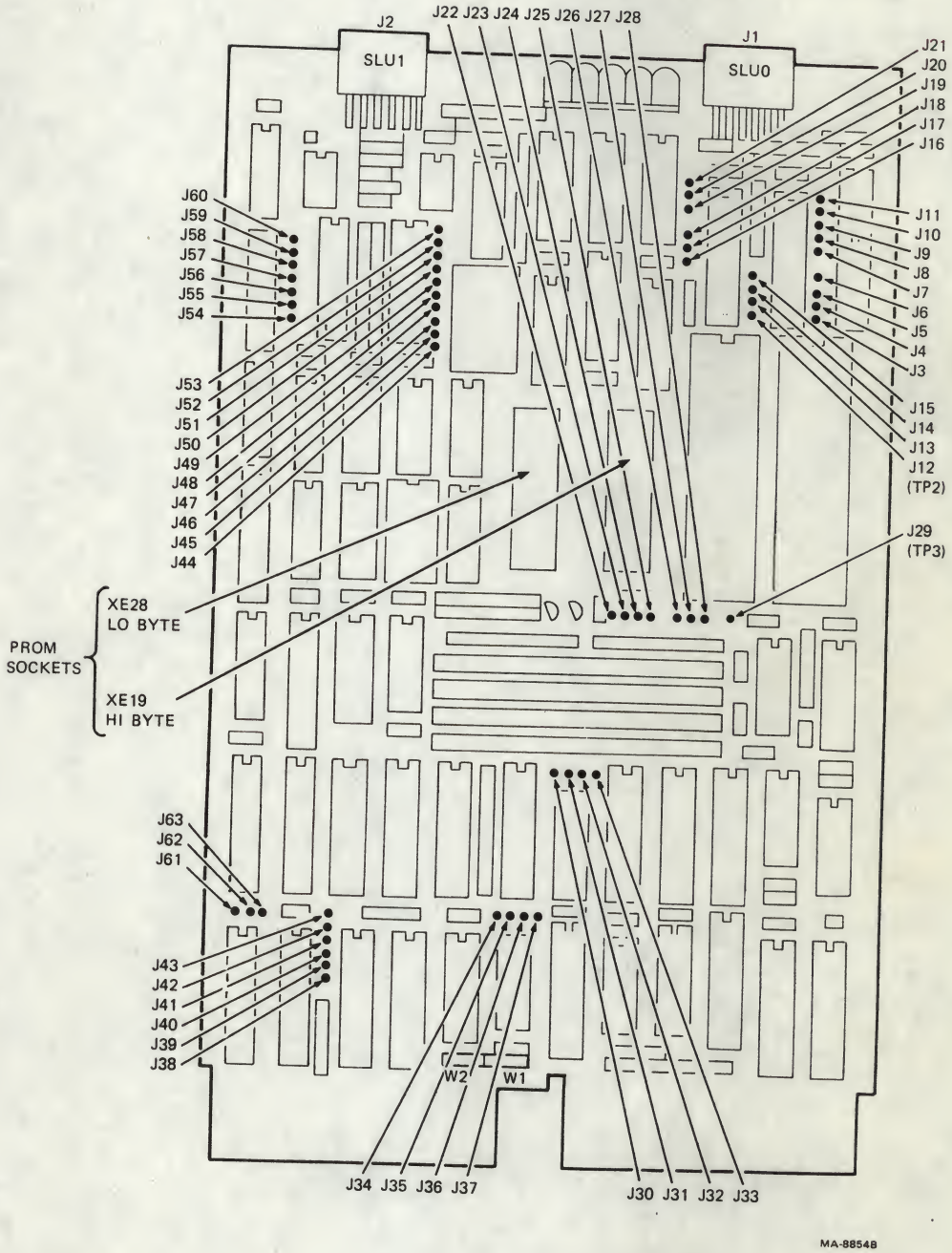


Figure 3-2 MXV11-B Jumper Locations

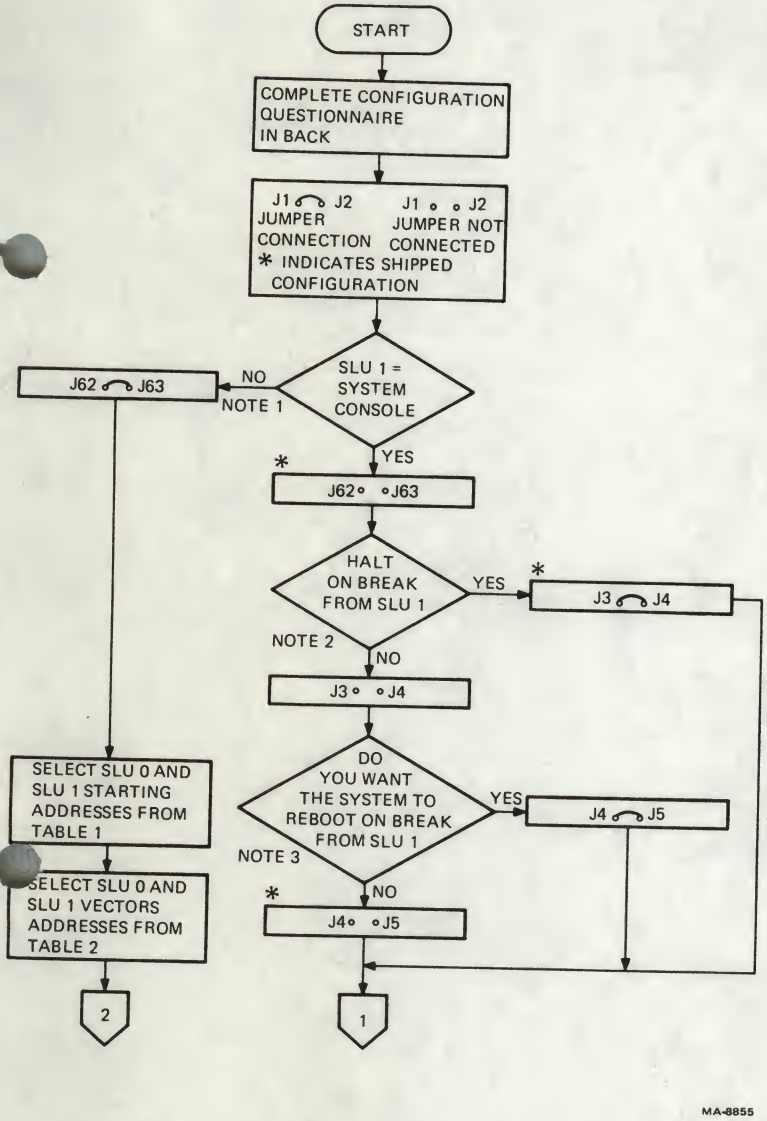
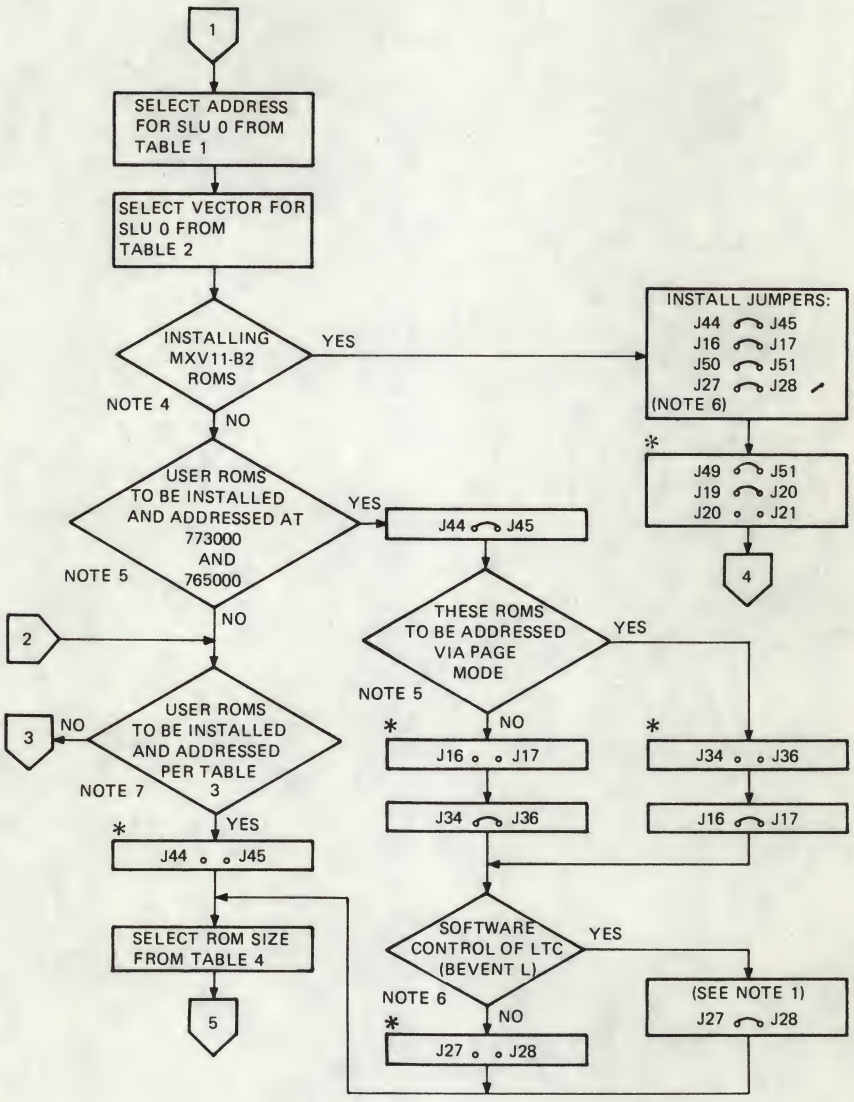


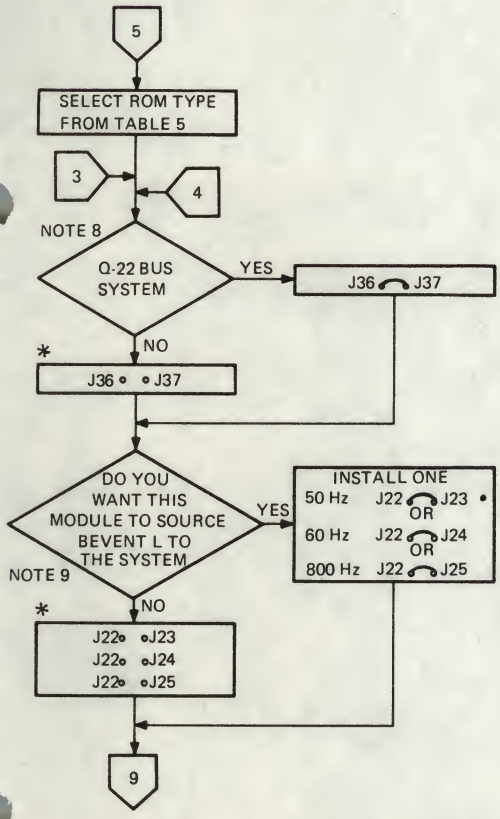
Figure 3-3 Jumper Configuration Flow Diagram (Sheet 1)



NOTE:
REFER TO NOTES IMMEDIATELY FOLLOWING THIS DIAGRAM.

MA-8856

Figure 3-3 Jumper Configuration Flow Diagram (Sheet 2)



NOTE: REFER TO NOTES IMMEDIATELY FOLLOWING THIS DIAGRAM.

MA-8857

Figure 3-3 Jumper Configuration Flow Diagram (Sheet 3)

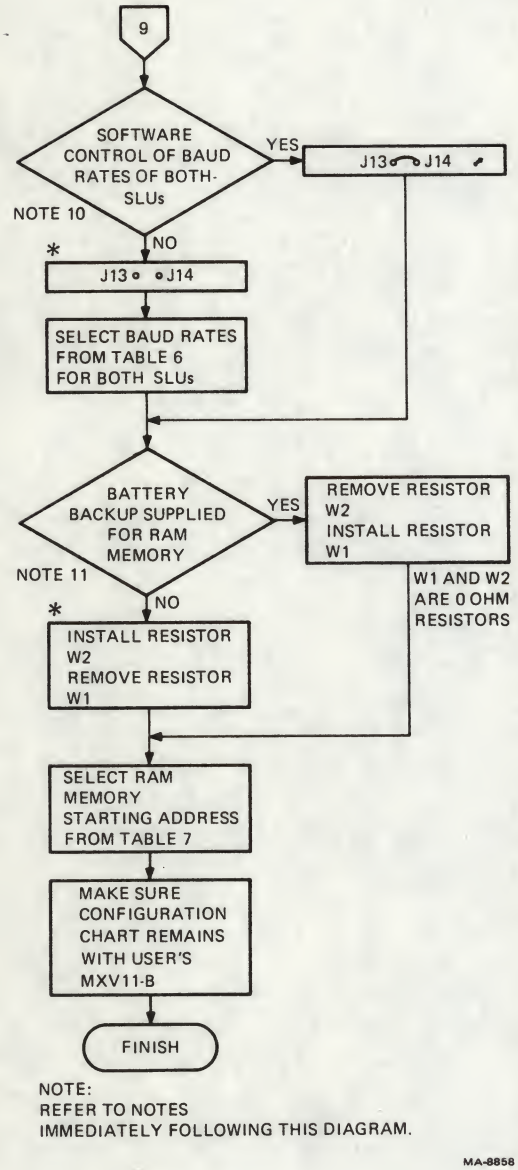


Figure 3-3 Jumper Configuration Flow Diagram (Sheet 4)

FIGURE NOTES

1. If SLU1 is not selected to be the system console (jumper installed from J62 to J63) the following features cannot be selected:

   Halt on break condition from SLU1 (never available with SLU0)
   Reboot on break condition from SLU1 (never available with SLU0)
   Console address (773000)
   MXV11-B2 ROMs or user ROMs addressed at 773000 and 765000
   Software control of the LTC (BEVENT L) (address 777546 does not exist)
   Page control register (address 777520 does not exist)
   Diagnostic display register (address 777524 does not exist)

2. A framing error or continuous spacing (break) condition from SLU1 will cause the BHALT L signal on the bus to be asserted by the MXV11-B causing the system to halt.

3. A framing error or continuous spacing (break) condition from SLU1 will cause the BDCLO L signal on the bus to be asserted by the MXV11-B and will cause the system to reboot if the CPU module is configured to do so.

4. MXV11-B2 ROMs are 8K × 8 UV PROMs and must have access to the page control register, diagnostic display register, and LTC control register.

5. User ROMs may be installed and addressed at 773000 and 776500. If more than 256 words are to be used in each address space, page mode must be enabled and addressing will be controlled by the page control register.

6. If control of LTC is selected (jumper installed from J27 to J28) the BEVENT L signal may be controlled by bit 06 in the LTC control register. If bit 06 is set, the BEVENT L signal on the bus will be driven by the source (usually by the power supply in Digital systems) allowing LTC interrupts. If bit 06 is reset, BEVENT L will be held low by the MXV11-B thereby inhibiting LTC interrupts.

CAUTION: Bit 06 is reset on power up. If another control register is included in the system (e.g., CPU module) and jumper J27 to J28 is installed, LTC interrupts will never be enabled because the LTC control register on the MXV11-B will not be accessed to set this bit.

7. User supplied ROMs are installed and addressed as memory residing in low memory space.

8. The MXV11-B may be installed in a Q-22 bus system or a Q-Bus system. If a jumper is not installed from J36 to J37 the RAM starting address is limited to 64K or below.

9. The MXV11-B can be configured to be the source of the BEVENT L signal for the system. Power supplies normally are the source of this signal in Digital systems. Do not have two sources in a system.

10. Baud rates for the serial lines may be software controlled or fixed by jumpers. If software control is desired, both SLUs will have this feature enabled and the fixed jumpers will have no effect.

11. Battery backup for the RAM memory and support circuits via pin AV1 on the backplane. Installing W1 and removing W2 removes normal system +5 V from the memory circuits only. Digital systems do not supply battery backup voltages to the backplane.

Table 3-1 summarizes all the jumpers on the MXV11-B module in numerical order. The jumpers are categorized by function and the connecting type is denoted by POC for push-on connector or WW for wire-wrap.

Table 3-1 Jumper Connections for MXV11-B

Jumper	Name	Function	Connection*
J1 •	Connector for SLU0		
J2 •	Connector for SLU1	SLU connectors	
J3 •	HALT		
J4 •	GND	Halt and reboot functions	POC (W3)
J5 •	RBOOT		
J6 •	OPEN		
J7 •	J1B		
J8 •	J1A	Serial line unit baud rates	WW
J9 •	GND		
J10 •	J0B		
J11 •	J0A		
J12 •	TP2	For engineering use	
J13 •	GND		
J14 •	SOFT EN	Software programmable	POC (W4)
J15 •	OPEN	baud rates	
J16 •	GND		
J17 •	PG L/DIR H	Enables or disables direct	POC (W5)
J18 •	OPEN	mode addressing	
J19 •	AL12H		
J20 •	NA12H	PROM size and type in	POC (W6)
J21 •	+5 V	direct mode addressing	
J22 •	LTC COMM		
J23 •	50 Hz	Line time clock frequency	WW
J24 •	60 Hz		
J25 •	800 Hz		
J26 •	OPEN		
J27 •	LTC EN IN	Software control of line	POC (W7)
J28 •	LTC EN OUT	time clock	

* POC = Push-on connector
WW = Wire-wrap

Note: W1 and W2 are 0 ohm resistors associated with battery backup option. Either one may be inserted but not both. The module is shipped with W2 inserted.

Table 3-1 Jumper Connections for MXV11-B (Cont)

Jumper	Name	Function	Connection*
J29 •	TP3	For engineering use	
J30 •	SLUA3		
J31 •	GND	Serial line unit starting address	WW
J32 •	SLUA2		
J33 •	SLUA1		
J34 •	DIR MODE BOOT		
J35 •	OPEN	Direct mode boot and small or large system	WW
J36 •	GND		
J37 •	SM/LG		
J38 •	JU1		
J39 •	JU2		
J40 •	GND	Serial line unit vector address	WW
J41 •	JL1		
J42 •	JL2		
J43 •	JL3		
J44 •	BOOT L/PROM H		
J45 •	GND	Boot ROM or user ROM	POC (W9)
J46 •	OPEN		
J47 •	CLOCK IN		
J48 •	CLOCK OUT	Master clock	POC (W10)
J49 •	PROM 1		
J50 •	PROM 2		
J51 •	GND	PROM size and PROM start address	WW
J52 •	BSK1		
J53 •	BSK2		
J54 •	AJ13		
J55 •	AJ14		
J56 •	AJ15	RAM starting address	WW
J57 •	GND		
J58 •	AJ16		
J59 •	AJ17		
J60 •	AJ18		
J61 •	OPEN		
J62 •	GND	Console mode	POC (W8)
J63 •	CONSOLE		

* POC = Push-on connector
WW = Wire-wrap

Note: W1 and W2 are 0 ohm resistors associated with battery backup option. Either one may be inserted but not both. The module is shipped with W2 inserted.

Table 3-2 contains the following jumper configurations.

Console mode
MXV11-B2 Boot ROM set
System size
Boot and diagnostic ROMs
Clock
Halt
Reboot
Line time clock
EVENT line
Software programmed baud rates
Battery backup
User-supplied ROMs

Table 3-2 Miscellaneous Jumper Configurations

NOTE: MXV11-B is shipped with jumpers disconnected unless otherwise specified.

Connector		Connection	Description
J63 • J62 • J61 •	CONSOLE GND OPEN	GND to OPEN (J62 to J61)	Enables console mode. SLU1 is fixed at address 777560 and vector address at 60. Select SLU 0 Address from Table 3-5 and vector from Table 3-6.
J63 • J62 • J61 •	CONSOLE GND OPEN	CONSOLE to GND (J63 to J62)	Disables console mode. For SLU addresses, refer to Table 3-5 and vectors from Table 3-6.
J46 • J45 • J44 •	OPEN GND BOOT L/PROM H	BOOT L/PROM H to GND (J44 to J45)	Inserted when MXV11-B2 Boot ROM set is installed in sockets XE19 and XE28. Enables the following registers to be addressed if the console GND to OPEN jumper (J62 to J61) is installed: Page control register Line time clock control Diagnostic display register.
J46 • J45 • J44 •	OPEN GND BOOT L/PROM H	GND to OPEN (J45 to J46)	Inserted when ROMs are for user code (not bootstrap code). See Table 3-3 for addresses.
J37 • J36 • J35 •	SM/LG SYS GND OPEN	SM/LG SYS to GND (J37 to J36)	Installed when the MXV11-B is connected in a Q22 bus backplane. Recognizes BDAL <21:00> L. This jumper must be installed if RAM is addressed above 128K words.

Table 3-2 Miscellaneous Jumper Configurations (Cont)

Connector		Connection	Description
J37 • J36 • J35 •	SM/LG SYS GND OPEN	GND to OPEN (J36 to J35)	Installed when the MXV11-B is connected to a 16-bit or 18-bit Q-bus. Recognizes BDAL <17:00> L only.
J36 • J35 • J34 •	GND OPEN DIRECT MODE BOOT	DIR MODE BOOT to OPEN (J34 to J35)	Module not wired for direct mode boot.
J36 • J35 • J34 •	GND OPEN DIRECT MODE BOOT	DIR MODE BOOT to GND (J34 to J36)	Module enabled for direct mode boot. This jumper must be installed when the user boot ROM is directly addressed.
J18 • J17 • J16 •	OPEN PG L/DIR H GND	PG L/DIR H to GND (J17 to J16)	Enables ROM boot map option and page mode on the MXV11-B. Disables user PROM addresses below 16K.
J18 • J17 • J16 •	OPEN PG L/DIR H GND	PG L/DIR H to OPEN (J17 to J18)	Enables PROM sockets XE19 and XE28 to be used for user defined PROMs. In this case, these sockets can only be addressed in memory locations below the 16K word boundary.
J48 • J47 •	CLOCK OUT CLOCK IN	CLOCK OUT to CLOCK IN (J48 to J47)	Factory test. Do not remove. This is the master clock, and provides on-board refresh and the charge pump to generate –12 V.
J3 • J4 • J5 • J6 •	HALT GND RBOOT OPEN	HALT to GND (J3 to J4)	Enables SLU 1 (console port) to halt the processor upon receiving a break character.

NOTE: HALT to GND (J3 to J4) and RBOOT to GND (J5 to J4) cannot be simultaneously jumpered.

J3 • J4 • J5 • J6 •	HALT GND RBOOT OPEN	HALT not connected to GND	Disables CPU halt function.
J3 • J4 • J5 • J6 •	HALT GND RBOOT OPEN	RBOOT to GND	Causes a system reboot when a break condition is received from SLU 1. Forces BDC OK-H low on the bus.

NOTE: HALT to GND (J3 to J4) and RBOOT to GND (J5 to J4) cannot be simultaneously jumpered.

Table 3-2 Miscellaneous Jumper Configurations (Cont)

Connector	Connection	Description
J3 • HALT J4 • GND J5 • RBOOT J6 • OPEN	GND to OPEN (J4 to J3)	Disables reboot function.
CAUTION: LTC EN IN to LTC EN OUT (J27 to J28) should not be connected if the CPU has an LTC control register.		
J26 • OPEN J27 • LTC EN IN J28 • LTC EN OUT	LTC EN IN to LTC EN OUT (J27 to J28)	Allows LTC to be software controlled. Enables control of BEVENT L on the bus via bit 06 of the LTC register. When bit 6 of LTC register is 0, BEVENT L will be asserted constantly low. This inhibits LTC interrupts. To address the LTC register (777546), the MXV11-B must be in boot mode (BOOT L/PROM H to GND) (J44 to J45) and SLU1 must be the console port (CONSOLE to GRD removed).
J26 • OPEN J27 • LTC EN IN J28 • LTC EN OUT	LTC EN IN to OPEN (J27 to J26)	Prevents bit 06 of the LTC register from controlling the BEVENT L line.
J22 • LTC COMM J23 • 50 Hz	LTC COMM to 50 Hz (J22 to J23)	When installed, the BEVENT line is driven from a 50 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.
J24 • 60 Hz	LTC COMM to 60 Hz (J22 to J24)	When installed, the BEVENT line is driven from a 60 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.
J25 • 800 Hz	LTC COMM to 800 Hz (J22 to J25)	When installed, the BEVENT line is driven from a 800 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.

NOTE: One of these jumpers (50, 60, or 800 Hz) should be installed: 1) If no external BEVENT source is provided in the system, and 2) If the user desires this source. Power supplies manufactured by Digital normally supply BEVENT L to the backplane.

Table 3-2 Miscellaneous Jumper Configurations (Cont)

Connector	Connection	Description
J15 • OPEN J14 • SOFT EN J13 • GND	SOFT EN to GND (J14 to J13)	Enables software programmable baud rates for both SLU1 and SLU0 via the CSR. The baud rate jumpers in Table 3-5 have no effect if the PBRE bit is set.
J15 • OPEN J14 • SOFT EN J13 • GND	SOFT EN to OPEN (J14 to J15)	Baud rates are selected from Table 3-5.
W1	W1 (0 ohm resistor) connected	Battery backup. +5B is supplied by user on backplane pin AV1. DEC does not supply battery backup.
W2	W2 (0 ohm resistor) connected	No battery backup.
J21 • +5 V J20 • NA12H J19 • BA12H	NA12H to +5 V (Normalized address 12) (J20 to J21) to (Buffered Address line 12)	Specifies 2K user UVROMs (2716) installed and direct mode addressing.
J21 • +5 V J20 • NA12H J19 • BA12H	NA12H to BA12H (J20 to J19)	Specifies 4K or 8K user-supplied ROM in direct mode addressing.

NOTE: There are cases where none of these jumpers (+5 V, NA12H, and BA12H) should be connected. In these cases, the push-on connector must be completely removed or must be connected to one of the outside pins to hold the connector. There is no open pin associated with these jumpers. For example, if 2K non-UV PROMs or the MXV11-B2 ROM is to be installed, these jumpers are all disconnected.

Tables 3-3 through 3-9 contain the following jumper configurations.

Table 3-3	PROM starting address
Table 3-4	SLU baud rates
Table 3-5	SLU starting address
Table 3-6	SLU vector address
Table 3-7	RAM starting address
Table 3-8	PROM address mode jumpers
Table 3-9	PROM size
Table 3-10	PROM size in user mode
Table 3-11	PROM size in boot mode (page addressing)
Table 3-12	PROM size in boot mode (direct addressing)

Table 3-3 Jumpers for PROM Starting Address

J51 • GND
J52 • BSK1
J53 • BSK2

BSK2 to GND (J53 to J51)	BSK1 to GND (J52 to J51)	User PROM Starting Address (octal) (See Note)
R	R	000000*
R	I	020000
I	R	040000
I	I	060000

R = jumper removed
I = jumper inserted to ground

Note: These addresses are for user supplied ROMs only. Jumpers BOOT L/PROM H to GND (J44 to J45) and PG L/DIR H to GND (J17 to J16) must be removed.

* Shipped configuration. Remove all jumpers from BSK1 (J52) and BSK2 (J53) if not in user mode.

Table 3-4 Serial Line Unit Baud Rates

		SLU0 (See Note)		
		J0B to GND (J10 to J9)	**J0A to GND (J11 to J9)**	**Baud Rates**
J11 •	J0B	R	R	300*
J10 •	J0B	R	I	1200
J9 •	GND	I	R	9600
		I	I	38.4K

		SLU1 (See Note)		
		J1A to GND (J8 to J9)	**J1B to GND J7 to J9)**	**Baud Rates**
J9 •	GND	R	R	9600*
J8 •	J1A	R	I	38.4K
J7 •	J1B	I	R	300
		I	I	1200

R = jumper removed
I = jumper inserted to ground

Note: SOFT EN to GND jumper (J14 to J13) must be removed; otherwise these jumpers have no effect. If the SOFT EN to GND jumper (J14 to J13) is installed and PBRE bit 1 is set, baud rates are software controlled.

* Shipped configuration

Table 3-5 Serial Line Unit Starting Address Jumpers

		SLUA3 to GND (J30 to J31)	**SLUA2 to GND (J32 to J31)**	**SLU1 to GND (J33 to J31)**	**Starting Address SLU0**	**SLU1 (See Note)**
J33 •	SLUA1	R	R	R	776500*	776510*
J32 •	SLUA2	R	R	I	776510	776520
J31 •	GND	R	I	R	776520	776530
J30 •	SLUA3	R	I	I	776530	776540
		I	R	R	776540	776550
		I	R	I	776550	776560
		I	I	R	776560	776570
		I	I	I	776570	776600

R = jumper removed
I = jumper inserted to ground

Note: If the GND to OPEN jumper (J62 to J61) is installed (console enabled), the SLU1 address is fixed at the standard console address of 777560 and this column does not apply.

* Shipped configuration

Table 3-6 Jumpers for SLU Vector Addresses

J43 • JL3
J42 • JL2
J41 • JL1
J40 • GND
J39 • JU2
J38 • JU1

JU2 to GND (J39 to J40)	JU1 to GND (J38 to J40)	JL3 to GND (J43 to J40)	JL2 to GND (J42 to J40)	JL1 to GND (J41 to J40)	SLU0	SLU1 (See Note)
R	R	R	R	R	300*	310*
R	R	R	R	I	010	020
R	R	R	I	R	020	030
R	R	R	I	I	030	040
R	R	I	R	R	040	050
R	R	I	R	I	050	060
R	R	I	I	R	060	070
R	R	I	I	I	070	100
R	I	R	R	R	100	110
R	I	R	R	I	110	120
R	I	R	I	R	120	130
R	I	R	I	I	130	140
R	I	I	R	R	140	150
R	I	I	R	I	150	160
R	I	I	I	R	160	170
R	I	I	I	I	170	200
I	R	R	R	R	200	210
I	R	R	R	I	210	220
I	R	R	I	R	220	230
I	R	R	I	I	230	240
I	R	I	R	R	240	250
I	R	I	R	I	250	260
I	R	I	I	R	260	270
I	R	I	I	I	270	300
I	I	R	R	R	300	310
I	I	R	R	I	310	320
I	I	R	I	R	320	330
I	I	R	I	I	330	340
I	I	I	R	R	340	350
I	I	I	R	I	350	360
I	I	I	I	R	360	370
I	I	I	I	I	370	Undefined

I = jumper inserted from specified pin to ground. Where multiple connections are made, they are daisy-chained.
R = jumper removed

Note: If the GND to OPEN jumper (J62 to J61) is installed (console enabled), SLU1 vector address is fixed at 60 and this column does not apply.

* Shipped configuration

Table 3-7 RAM Starting Address Jumpers

J60 • AJ18
J59 • AJ17
J58 • AJ16
J57 • GND
J56 • AJ15
J55 • AJ14
J54 • AJ13

	AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
00	R	R	R	R	R	R	0*
01	R	R	R	R	R	I	4K
02	R	R	R	R	I	R	8K
03	R	R	R	R	I	I	12K
04	R	R	R	I	R	R	16K
05	R	R	R	I	R	I	20K
06	R	R	R	I	I	R	24K
07	R	R	R	I	I	I	28K
10	R	R	I	R	R	R	32K
11	R	R	I	R	R	I	36K
12	R	R	I	R	I	R	40K
13	R	R	I	R	I	I	44K
14	R	R	I	I	R	R	48K
15	R	R	I	I	R	I	52K
16	R	R	I	I	I	R	56K
17	R	R	I	I	I	I	60K
20	R	I	R	R	R	R	64K
21	R	I	R	R	R	I	68K†
22	R	I	R	R	I	R	72K†
23	R	I	R	R	I	I	76K†
24	R	I	R	I	R	R	80K†
25	R	I	R	I	R	I	84K†
26	R	I	R	I	I	R	88K†
27	R	I	R	I	I	I	92K†
30	R	I	I	R	R	R	96K†
31	R	I	I	R	R	I	100K†
32	R	I	I	R	I	R	104K†
33	R	I	I	R	I	I	108K†
34	R	I	I	I	R	R	112K†
35	R	I	I	I	R	I	116K†
36	R	I	I	I	I	R	120K†
37	R	I	I	I	I	I	124K†
40	I	R	R	R	R	R	128K†
41	I	R	R	R	R	I	132K†
42	I	R	R	R	I	R	136K†
43	I	R	R	R	I	I	140K†
44	I	R	R	I	R	R	144K†
45	I	R	R	I	R	I	148K†
46	I	R	R	I	I	R	152K†
47	I	R	R	I	I	I	156K†
50	I	R	I	R	R	R	160K†
51	I	R	I	R	R	I	164K†
52	I	R	I	R	I	R	168K†
53	I	R	I	R	I	I	172K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.
R = jumper removed.

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

Table 3-7 RAM Starting Address Jumpers (Cont)

	AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
54	I	R	I	I	R	R	176K†
55	I	R	I	I	R	I	180K†
56	I	R	I	I	I	R	184K†
57	I	R	I	I	I	I	188K†
60	I	I	R	R	R	R	192K†
61	I	I	R	R	R	I	196K†
62	I	I	R	R	I	R	200K†
63	I	I	R	R	I	I	204K†
64	I	I	R	I	R	R	208K†
65	I	I	R	I	R	I	212K†
66	I	I	R	I	I	R	216K†
67	I	I	R	I	I	I	220K†
70	I	I	I	R	R	R	224K†
71	I	I	I	R	R	I	228K†
72	I	I	I	R	I	R	232K†
73	I	I	I	R	I	I	236K†
74	I	I	I	I	R	R	240K†
75	I	I	I	I	R	I	244K†
76	I	I	I	I	I	R	248K†
77	I	I	I	I	I	I	252K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.
R = jumper removed.

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

NOTE: Be careful when configuring the MXV11-B RAM when ROM is used in the USER ROM address space. USER ROM address space is defined as bus addresses 0–16K, (00000–100000) on 4K boundaries. The RAM start address must be higher than the last location of the ROM or dual responses from both the RAM and ROM will occur. The chart below shows several examples of right and wrong ways of assigning RAM memory start addresses.

ROM Size	ROM Start	RAM Start	RAM End	Comments
8K	0K	4K	68K	Wrong, 4K overlap (4K→8K)
8K	4K	0K	64K	Wrong, 8K overlap (4K→12K)
4K	0K	4K	68K	Right, no overlap
4K	0K	12K	76K	Right, no overlap‡
8K	4K	12K	76K	Right

‡ Address space gap usually not recommended but up to user to decide depending on application.

Table 3-8 PROM Jumpers

J19 • BA12H
J20 • NA12H
J21 • +5 V

NA12H to BA12H (J20 to J19)	NA12H to +5 V (J20 to J21)	Description
R	R	Page mode – Boot ROM for 2K by 8 non-UV PROMs, 4K by 8 or 8K by 8 PROMs
I	R	Direct mode – for 2K by 8, non-UV PROMs, 4K by 8, or 8K by 8 PROMs.*
R	I	Direct mode – for 2K by 8 UV PROMs.

R = jumper removed
I = jumper inserted

* Shipped configuration

Table 3-9 Jumpers to Configure PROM Size

J51 • GND
J50 • PROM 2
J49 • PROM 1

PROM 2 To GND (J50 to J51)	PROM 1 To GND (J49 to J51)	PROM Size
R	R	No ROMs*
R	I	2K by 8
I	R	4K by 8
I	I	8K by 8†

R = jumper removed
I = jumper inserted

* Shipped configuration. Additional jumpers are required depending on user mode/boot mode and direct addressing page addressing. Refer to Tables 3-10, 3-11, and 3-12.

† If the MXV11-B2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND jumper (J50 to J49 to J51).

3.2 JUMPER CONFIGURATIONS

The MXV11-B module is shipped with jumpers connected in the default condition listed below. The default configuration generally has no jumpers installed, and push-on connectors are connected to the open pins.

SLU 0

Address	776500
Vector	300
Baud rate	300

SLU 1

Address	777560
Vector	60
Baud rate	9600

Halt on Break from SLU 1 – enabled
Reboot on Break from SLU 1 – disabled

Line time clock (LTC) control register address 777546 – disabled.

Page control register (PCR) address 777520 – disabled.

Diagnostic display register address 777524 – disabled.
ROM size – no ROMs
ROM starting address – 000000
BEVENT L – not driven by this module

Q-22 Bus or Q-bus – Q-bus enabled

Software controlled baud rates for SLU 1 and SLU 0 – disabled

RAM starting address – 000000

The following jumpers use push-on connectors and are listed in the configuration in which they are shipped from the factory. All other jumpers are wire-wrapped.

- CLK IN to CLK OUT – J47 to J48 (W10) – master clock, –12 V and on-board refresh
- GND to OPEN – J45 to J46 (W9) – user mode
- PG L/DIR H to OPEN – J17 to J18 (W5) – page mode disabled
- SOFT EN to OPEN – J14 to J15 (W4) – baud rates under hardware control

- RBOOT to OPEN – J5 to J6 (W3) – no boot or halt on break
- LTC EN IN to OPEN – J27 to J26 (W7) – no line time clock clamp; MXV11-B does not control BEVENT.
- BA12H to NA12H – J19 to J20 (W6) – direct mode address 12 supplied to ROM sockets (4K by 8, 8K by 8 ROMs).
- GND to OPEN – J62 to J61 (W8) – SLU 1 acts as system console port

Figure 3-3 is a flow diagram which provides a detailed method of configuring the jumpers on the MXV11-B module for the user's specific application. Asterisks on the diagram indicate the jumper configuration of the module when it is shipped from the factory. Sometimes, the flow diagram refers to tables in this chapter which indicate the shipped configuration. It is important to note that certain jumpers must not be connected for specific functions.

The flow diagram contains paragraph references. These references point the reader to additional information. The diagram includes a series of numbers in parenthesis and preceded by the word "note." These numbers refer to a set of notes immediately following the diagram. The notes provide further information.

3.3 ROM CONFIGURATIONS

The MXV11-B contains two 28-pin sockets to house the ROMs. The sockets can support 2K by 8, 4K by 8, or 8K by 8 ROMs which may contain bootstrap code, diagnostic code, or user code.

The 2K by 8 and 4K by 8 PROMs each contain 24 pins while the 8K by 8 PROM contains 28 pins. Figure 3-4 shows the Intel configuration for each size PROM.

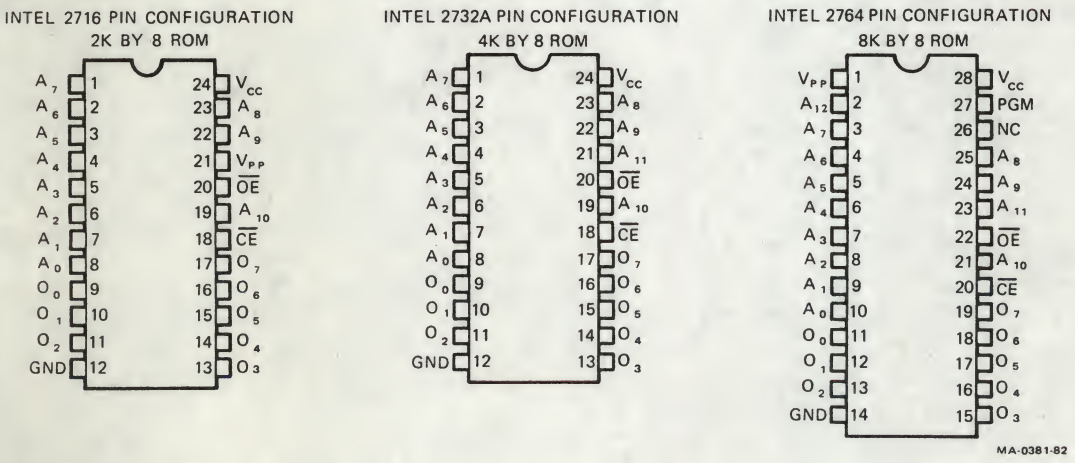


Figure 3-4 PROM Chips

Use this configuration or equivalent. For example, the Intel 2716 PROM chip is a 2K by 8 UVPROM. A similar PROM chip, compatible with the 2716, may be used as a 2K by 8 PROM.

NOTE: The MXV11-B supports INTEL 2716, 2732, 2732A, 2764 UVPROMS.

When you install a 2K by 8 or 4K by 8 PROM in the 28-pin PROM sockets (XE28 for low byte or XE19 for high byte), you must install the 24-pin PROM in the 28-pin socket with the notch on top, pin side down, and bottom justified. This means you insert pin 1 of the PROM chip in pin 3 of the PROM socket (Figure 3-5).

For the 28-pin PROM chip, pin 1 of the chip is plugged into pin 1 of the socket with the notch on the top and pin side down.

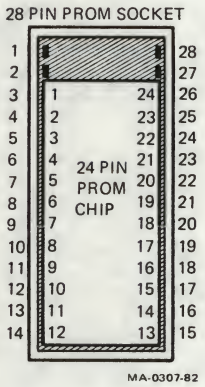


Figure 3-5 Insertion of 24-Pin PROM Chips

3.3.1 User Mode (Direct Addressing)

Table 3-10 shows the jumper connections for the various PROM sizes in user mode. The MXV11-B module must be configured for no PROMs if PROMs are not inserted in the sockets.

Table 3-1 summarizes all the jumpers on the module. Blank lines separate the jumpers functionally.

NOTE: Page mapping is not available in user mode.

3.3.2 Boot Mode (Page Addressing)

Table 3-11 shows the jumper connections for the various PROM sizes in boot mode using page mode addressing. The MXV11-B module must be configured for no PROMs if PROMs are not inserted in the sockets.

Table 3-10 Jumper Connections for PROM Sizes in User Mode

	No PROMs	2K by 8	4K by 8	8K by 8
J16 • (GND) J17 • (PG L/DIR H) J18 • (OPEN)	J17 to J18	J17 to J18	J17 to J18	J17 to J18
J19 • (BA12H) J20 • (NA12H) J21 • (+5 V)	J19 to J20	J20 to J21	J19 to J20	J19 to J20
J44 • (BOOT L/PROM H) J45 • (GND) J46 • (OPEN)	J45 to J46	J45 to J46	J45 to J46	J45 to J46
J49 • (PROM1) J50 • (PROM2) J51 • (GND)	–	J49 to J51	J50 to J51	J49 to J50 to J51

Note: Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J45 is connected to J46, and J49 is connected to J51.

Table 3-11 Jumper Connections for PROM Sizes in Boot Mode (Page Addressing)

	No PROMs	2K by 8*	4K by 8	8K by 8
J16 • (GND) J17 • (PG L/DIR H) J18 • (OPEN)	J17 to J18	J16 to J17	J16 to J17	J16 to J17
J19 • (BA12H) J20 • (NA12H) J21 • (+5 V)	J19 to J20	–	J19 to J20	J19 to J20
J44 • (BOOT L/PROM H) J45 • (GND) J46 • (OPEN)	J45 to J46	J44 to J45	J44 to J45	J44 to J45
J49 • (PROM1) J50 • (PROM2) J51 • (GND)	–	J49 to J51	J50 to J51	J49 to J50 to J51

* 2K by 8 UV PROM cannot be used in page mode.

Note: Jumper connections are indicated. For example, in the 8K by 8 PROM, J16 is connected to J17, J19 is connected to J20, J44 is connected to J45 and J49, J50 and J51 are connected.

3.3.3 Boot Mode (Direct Addressing)

Table 3-12 lists the jumper connections for the various PROM sizes in boot mode using direct addressing. The MXV11-B module must be configured for no PROMs if PROMs are not inserted in the sockets.

3.4 SLU CONFIGURATIONS

If you want to use one of the SLUs as a console, you must connect the console terminal to SLU 1 since the halt on break, reboot on break, console address, and vector functions are only selectable for use with SLU 1. To halt on break the HALT to GND jumper must be connected. When connected, the CPU halts on a break from the SLU. The break could be the result of a framing error or an operator request. To reboot on a break condition, connect the RBOOT to GND jumper.

In console mode, the SLU 1 address is fixed at 777560 and the SLU 1 vector address is fixed at 60. The SLU 0 address is selected from Table 3-5 and the SLU 0 vector is selected from Table 3-6.

Table 3-12 Jumper Connections for PROM Sizes in Boot Mode (Direct Addressing)

	No PROMs	2K by 8	4K by 8	8K by 8
J16 • (GND) J17 • (PG L/DIR H) J18 • (OPEN)	J17 to J18	J17 to J18	J17 to J18	J17 to J18
J19 • (BA12H) J20 • (NA12H) J21 • (+5 V)	J19 to J20	J20 to J21	J19 to J20	J19 to J20
J44 • (BOOT L/PROM H) J45 • (GND) J46 • (OPEN)	J45 to J46	J44 to J45	J44 to J45	J44 to J45
J49 • (PROM1) J50 • (PROM2) J51 • (GND)	–	J49 to J51	J50 to J51	J49 to J50 to J51
J34 • (DIR MODE BOOT) J35 • (OPEN) J36 • (GND)	–	J34 to J36	J34 to J36	J34 to J36

Note: Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J44 is connected to J45, J49 is connected to J51, and J34 is connected to J36.

With the SOFT EN to OPEN jumper (J14 to J15) connected, the baud rates are hardware controlled (strapped) by inputs to the DLART (Table 3-4). If the SOFT EN to GND jumper (J14 to J13) is connected, the baud rate selection from Table 3-4 is disabled and software controlled baud rates for both SLUs are enabled. To use software controlled baud rates, software must write the XCSR register of the desired SLU in the following manner. First, the programmable baud rate enable bit (PBRE–bit 1 of XCSR) must be set. If this bit is not set, the fixed hardware inputs will control the baud rates. Second, the programmable baud rate bits (bits PBR 2, 1, and 0 in the XCSR) must be set in the proper configuration for the desired baud rates (Paragraph 2.6.4).

If SLU 1 is selected for console mode, it uses the hardware inputs to select the baud rates. Since the SOFT EN to GND jumper (J14 to J13) enables software baud rates for both SLUs, PBRE bit 1 in the XCSR of SLU 1 must be reset. It is possible to have SLU 0 operate with software controlled inputs by setting the PBRE bit in the SLU 0 XCSR to a 1 and configuring the PBR bits in that XCSR to the desired baud rate.

NOTE: If a power-down or power-up bus reset or initialize occurs, the XCSR registers are cleared and the baud rate is reset to 300 baud. So it is necessary to reset the bits in the XCSR registers to the previous configuration.

3.5 LINE TIME CLOCK CONTROL

Line time clock (LTC) interrupts can be enabled or disabled by the LTC IN and LTC OUT jumpers and by the state of bit 6 of the LTC control register.

If the LTC EN IN to LTC EN OUT jumper (J27 to J28) is connected, BEVENT L is asserted constantly low on the bus provided bit 06 of the LTC control register is reset. This disables LTC interrupts in the system. When bit 06 is set, BEVENT L (if selected as the source) is allowed to be driven by the MXV11-B at a frequency of 50, 60, or 800 Hz. Digital power supplies and backplanes normally supply a line time clock for the system. Do not have two sources in the system.

To address the LTC control register, the BOOT L/PROM H to GND jumper (J44 to J45) and the GND to OPEN jumper (J62 to J61) must be connected. If the BOOT L/PROM H to OPEN jumper (J44 to J46) is connected or the CONSOLE to GND (J63 to J62) jumper is connected, the LTC CSR cannot be accessed by the system.

If the LTC EN IN to OPEN jumper (J27 to J26) is connected, BEVENT L is not controlled by the LTC register.

3.6 LTC FREQUENCY

The LTC can be selected to operate at 50, 60, or 800 Hz by driving the BEVENT L line at the desired frequency (refer to Table 3-2).

4

MAINTENANCE AND DIAGNOSTICS

4.1 GENERAL

This chapter describes the maintenance and diagnostic for the MXV11-B module. The MXV11-B CVMX BAO diagnostic tests the module. It verifies:

Operation of the two serial line units
Read only memory option (ROM)
Clock option
Page control register (PCR)
Diagnostic display register (DDR)
Random access memory (RAM).

The diagnostic runs on any Q-bus PDP-11 with 16K words of memory. It runs under XXDP+ and APT monitors and on processors with no hardware switch register.

NOTE: CPUs without memory management (LSI or LSI/2) cannot test all of the MXV11-B's memory. These systems can only verify/test the lower 32K words (actually 32K words minus the I/O page, i.e., lower 28K). CPUs with memory management can check up to two MXV11-B modules minus the I/O page, i.e., 124K words.

The program tests whatever options the device map ($DEVM) is set to, prints the contents of the device map for operator verification, and also prints a summary of significant differences from the default conditions. For example, differences might be channel(s) dropped from testing, using channel 1 as console, or bypassing ROM and RAM testing.

4.2 DATA TESTING

Data testing of the DLART is done by internal wrap. This checks out the DLART only and not the complete functionality of the SLU. To check out the SLU, external wraparound connectors are required so that the receiver and transmitter chips may be tested.

4.3 SERIAL LINE UNIT TESTING

Serial line unit testing is done in two distinct phases:

1. Each of the two MXV11-B channels is tested individually.
2. The MXV11-B module is tested as a whole for channel interaction problems. This diagnostic is designed to test and detect errors to the logic level and not the chip level.

The addresses and vector ranges are as follows.

Channel 0	776500–776570	
Channel 1	776510–776600	777560 (as console)
Vectors	004–376	
PCR	777520	
DDR	777524	
LTC	777546	

The default addresses and vectors are as follows.

Channel 0	776500–776506	Vectors 300/304
Channel 1	777560–777566	Vectors 60/64

For any other device addresses the operator must change the default locations. (See program options and defaults in Paragraph 4.4.)

4.4 PROGRAM OPTIONS AND DEFAULTS

The MXV11-B diagnostic needs the address of the first RCSR of each SLU and its interrupt vectors to be previously stored unless the default address and vector is desired.

NOTE: The test can be run with one MXV11-B in which case channels 0 and 1 apply; or it can be run with two MXV11-Bs and channels 0–3 apply.

		Diagnostic Location	Address/Vector	
One MXV11-B	Channel 0	1254	776500	RCSR 1
		1256	300	Vector
	Channel 1	1260	777560	RCSR 2
		1262	60	Vector
Two MXV11-Bs	Channel 2	1264	776510	RCSR 1
		1266	310	Vector
	Channel 3	1270	776520	RCSR 2
		1272	320	Vector

LOROM	1274	773000	Low ROM address
HIROM	1276	773776	High ROM address (256 words)
LOROM2	1300	765000	2nd low ROM address
HIROM2	1302	765776	2nd high ROM address (256 words)
BASE2	1264	776510	Channel 2
VECT2	1266	310	Channel 2
BASE3	1270	776520	Channel 3
VECT3	1272	320	Channel 3

Location '$DEVM' (default = 000000) is a bit map that shows which options are present and to be tested.

The operator is prompted on initial program startup.

'$DEVM' can be changed anytime by typing Control-G and Control-C. The program will resize and restart at the beginning again. The $DEVM can be found at location 1252.

Each bit of the device map ($DEVM) is briefly described below.

Bit 15

0 = test channel 0	= default
1 = bypass channel 0 test	= 100000

Bit 14

Not used

Bit 13

0 = test 1 MXV11-B module	= default
1 = test 2 MXV11-B modules	= 020000

Bit 12

0 = CPU has memory management	= default
1 = CPU has no MEM MNGT (LSI11/2)	= 10000

Bit 11

0 = break detection disabled	= default
1 = break detection enabled	= 4000

NOTE: Break detection is tested on channel 0 only.

Bit 10

0 = do data wraparound tests	= default
1 = bypass data wrap tests	= 2000

Bit 9

0 = do data wrap external tests	= default
1 = bypass wrap internal tests	= 1000

NOTE: This bit selection is only used if data wrap has already been selected via bit 10 or 3.

Bit 8

0 = bypass channel 1 test	= default
1 = test channel 1	= 400

Bit 7

0 = enable PCR register test	= default
1 = bypass PCR register test	= 200

Bit 6

0 = enable LEDs test # display	= default
1 = bypass use of LEDs	= 100

NOTE: The LED register is also called the DDR register.

Bit 5

Not used

Bit 4

0 = break detection disabled	= default
1 = break detection enabled	= 20

NOTE: Bit 4 affects channel 1 only.

Bit 3

0 = bypass data wrap tests	= default
1 = do data wraparound tests	= 10

NOTE: Bit 3 affects channel 1 only.

Bit 2

0 = test RAM	= default
1 = bypass RAM tests	= 4

Bit 1

0 = bypass ROM testing	= default
1 = ROM present (test)	= 2

Bit 0

0 = clock option disabled	= default
1 = clock option enabled	= 1

NOTE: CPUs without memory management (LSI or LSI/2) cannot test all of the MXV11-B's memory. These systems can only verify/test the lower 32K words (actually 32K words minus the I/O page, i.e., lower 28K). CPUs with memory management can check up to two MXV11-B modules minus the I/O page, i.e., 124K words.

4.5 EXECUTION TIMES

Execution times for an LSI-11 processor with the MXV11-B module at shipment configuration are listed below.

	LSI-11	F-11 (LSI-11/23)	
First pass	17 sec	08 sec	with one MXV11-B
Additional passes	45 sec	23 sec	with one MXV11-B
Channel 0		at 300 baud	
Channel 1 (console)		at 9600 baud	

The test time is baud rate dependent; higher baud rates result in shorter pass times.

The RAM tests require the additional times shown below for all passes.

	LSI-11	LSI-11/23 (64K words)	LSI-11/23 (124K words)
1st pass	4 sec	10 sec	19 sec
2nd pass	16 sec	10 sec	33 sec

4.6 POWER FAIL

Auto start from power fail is used in this program. Upon power up, the program restarts from the beginning.

4.7 ERROR HANDLING

Since this diagnostic was designed to fit in 16K of memory the error typeout is very brief. The format of the error typeout is as follows:

Test #_____,Error #_____,PC=_____,Address=_____,Vector=_____

where all values typed are octal. The address and vector refer to the failing channel. For further information the listing must be consulted. After an error is found, bits 15, 13, 10, and 9 of the switch register (SWREG) control the sequence of events as shown below.

Bit 15 set – makes the program halt in the error routine. If the program is continued, it proceeds from where it halted.

Bit 13 set – disables printing of the error message.

Bit 10 set – rings the bell on error.

Bit 9 set – makes the diagnostic loop from beginning of test to error.

The error routine supports the control G <^G> function. Refer to Paragraph 4.9.

The only halt in this diagnostic is in the error routine, and is executed only if bit 15 of the switch register (SWREG location 176) is set when an error occurs.

The error numbers have been updated to reflect the test they are called from. For example:

Error # 35 = Test 3, error number within the test is 5;

Error # 237 = Test 23, error number within the test is 7.

NOTE: All tests conform to this format except test 21. That test numbers its tests from 1 to 13 (octal).

4.8 DEVICE REGISTERS

The MXV11-B device registers and bit formats are shown in Appendix A.

4.9 SUMMARY OF TESTS AND SPECIAL SUBROUTINES

This paragraph briefly describes the various diagnostic tests.

PHASE 1 TESTS

Test 1 – RAM Address Test – writes the entire first 32K with the address of the location. It then checks the memory to be sure the write was correct. If an error occurs, and the program has been set up to halt, the failing address is in CPU register 0.

This test also checks for the presence of the DDR register. If the register "READ" creates a timeout an error will be generated.

Test 1 has errors 11 (data not = address) and 12 (LEDs not there).

Test 2 – RAM Data and Volatility Test – Write all memory to all 1s (background pattern).

1. Test location for correct pattern.
2. Float 0s and complement through word.
3. Reset location to all 1s.

Repeat above three steps for each location. When all locations are tested, check entire memory for background pattern. Repeat all the above for background pattern of all 0s and floating 1s. This test uses the memory management option. If a failure occurs examine CPU register R2. This register contains the failing 4K (octal) page number.

Test 2 has errors:

21 print "MEM BAD",
22 print "MEM BAD",
23 print "MEM BAD", and
24 print "MEM BAD".

Test 3 – ROM Tests – This is a two-part test. The first part checks the presence of addresses X73000–X73776. The second part checks the addresses of X65000–X65776.

This test also checks for the presence, if $DEVM selected, of the PCR register. If the register is present then it checks for a write of all 1s to the register. It then floats a one through a field of zeros.

Test 3 has errors:

31 bad address
32 RAM instead of ROM
33 bad address
34 RAM instead of ROM
35 trap occurred
36 PCR cannot hold all 1s
37 wrong bits appeared

Test 4 – Clock Tests – The clock test, if selected via the $DEVM, simply enables the clock and checks for an interrupt.

Test 4 has errors:

41 no clock interrupt, and
42 unexpected 2nd clock interrupt

NOTE: The following tests check both SLUs except for the case where the SLU is used as a console.

Test 5 – Addressability – Verifies that all eight registers of the channel under test respond to their addresses.

Test 5 has errors:

51 timeout on channel address
52 RCSR has unused bits set
53 RBUF has unused bits set
54 XCSR has unused bits set
55 XBUF has unused bits set

The following three tests test all 'read write' bits

Test 6 – Break (BK) – XCSR 0 reset, set, clear, reset

Test 6 has errors:

61 BK remained high
62 BK did not set in XCSR
63 BK did not clear in XCSR
64 BK did not reset in XCSR

Test 7 – Interrupt Enable (IE) – XCSR 6 reset, set, clear, reset

Test 7 has errors:

71 IE did not reset in XCSR
72 IE did not set in XCSR
73 IE did not clear in XCSR
74 IE did not reset in XCSR

Test 10 – Interrupt Enable (IE) – RCSR 6 reset, set, clear, reset

Test 10 has errors:

101 IE did not reset in RCSR
102 IE did not set in RCSR
103 IE did not clear in RCSR
104 IE did not reset in RCSR
105 TR not set

Test 11 – Transmitter Ready (TR) – XCSR 7 – clears when TBUF is loaded with a character and checks that it sets a reasonable amount of time.

Test 11 has errors:

111 TR did not set in XCSR
112 TR did not set in XCSR
113 TR did not clear in XCSR

Test 12 – Receiver Done (RD) – outputting a character from XBUF (with wraparound connected) results in RD setting a reasonable amount of time.

Test 12 has errors:

121 RD did not set in RCSR
122 RD did not reset in RCSR

Test 13 – Receiver Done (RD) – cleared by reading RBUF.

Test 13 has errors:

131 RD did not set in RCSR
132 RD did not clear in RCSR

Test 14 – Overrun (OE) and error bit (ER) – RBUF 14

Test 14 has errors:

141 RD did not set in RCSR
142 OE did not set in RBUF
143 ER did not set in RBUF
144 Reading RBUF cleared OE
145 RD did not set in RCSR
146 OE did not clear in RBUF
147 ER did not clear in RBUF

Test 15 – Transmitter interrupt logic test – checks transmitter interrupt logic by setting CPU priority to 0 in processor status word with interrupt enable (IE) set.

Test 15 has errors:

151 TR did not set in XCSR
152 interrupt flag did not set
153 XCSR sent second interrupt (unexpected)
154 interrupt flag occurred with IE disabled

Test 16 – Receiver interrupt logic test – covers all of the receiver side of the interrupt logic in character mode.

Test 16 has errors:

161 TR did not set in XCSR
162 interrupt flag did not set
163 RBUF sent second interrupt (unexpected)
164 interrupt flag occurred with IE disabled

Test 17 – Test data wraparound binary count: flag mode.

Test 17 has errors:

171 TR did not set in XCSR
172 RD did not set in XCSR
173 ER bit set in high byte of RBUF

Test 20 – Test data wraparound binary count: interrupt mode.

Test 20 has errors:

201 Hung, no data transfers
202 overrun error (OE)
203 framing error (FE)
204 not used presently
205 data compare error (received data did not compare with transmitted)

Test 21 – Test break logic: transmit known character – a) Transmit known character with break bit set and compare received character with 0. Received character should be 0. b) Test for framing error on break.

Test 21 has errors:

1 RD did not set in RCSR
2 BK failed to clear in RBUF
3 RD failed to set
4 Reset did not clear OE, FE in RBUF
5 BK error
6 Framing error (FE)
7 BK did not set in XCSR
10 RD did not set in RCSR
11 CHAR after BK not received correctly

Test 22 – Not a test – send back to loop.

PHASE 2 TESTS

Test 23 – test that channels interrupt at assigned priority

Test 23 has errors:

231 No RD
232 No RD
233 Did not interrupt at assigned priority
234 Did not interrupt at assigned priority
235 Did not interrupt at assigned priority
236 Did not interrupt at assigned priority
237 DONE failed to set after transmission of word

Test 24 – test data transfers with all active lines interrupting.

Test 24 has errors:

241 RD failed to set after transmission of word
242 ER flag after transfer
243 data compare error
244 ER flag up after transfer
245 data compare error

Test 25 – test that channels interrupt at assigned priority. This test is executed only on the second MXV11-B module (channels 2 and 3). Any failure is related to the second MXV11-B board.

Test 25 has errors:

251 No RD
252 No RD
253 did not interrupt at assigned priority
254 did not interrupt at assigned priority
255 did not interrupt at assigned priority
256 did not interrupt at assigned priority

Test 26 – test data transfers with all active lines interrupting. This test is executed only on the second MXV11-B module (channels 2 and 3). Any failure is related to the second MXV11-B board.

Test 26 has errors:

261 RD failed to set after transmit
262 ER flag after transfer
263 data compare error
264 ER flag after transfer
265 data compare error

4.10 SYSTEM REQUIREMENTS

The hardware system requirements are:

- KDF11, KDF11-B, KD11-HA, or KD11-F processors
- 16K word memory – minimum. A special data wraparound connector (PN 3270-A) is required if data wraparound tests are desired
- If channel 1 is the console, tests 11–14, 16–21, 23-24 are bypassed (bypass is for channel 1 only)
- If data wraparound tests are bypassed, tests 12–14, 16–21, 23-24 are bypassed.

The software system requirements are as follows.

This diagnostic can run in the following ways:

1. with APT monitor

2. with XXDP+ monitor (chainable if renamed to .BIC extension).

This diagnostic is not designed to run with the diagnostic supervisor.

It is assumed the operator must perform the following settings:

1. Set the software switch register (SWR) if not defaulted (Paragraph 4.4).

2. Set the device map ($DEVM) if not defaulted, (Paragraph 4.4).

3. Set the serial line addresses and vectors if not defaulted (Paragraph 4.4).

4. Set the ROM HI and LOW ADDR if not defaulted (Paragraph 4.4).

If channel 1 is configured as the console and the VT100 is the console device, "SETUP B" must be set for the following:

Disable XON/XOFF
Jump scroll ON
New line OFF
All other options per system requirements.

4.11 OPERATING INSTRUCTIONS

4.11.1 Loading and Starting Procedures

Use standard procedure for PDP-11 absolute binary formatted media.

All normal starts and restarts are from location 200.

There are two starting addresses to be used off-line only for interrupt vector troubleshooting:

1. 1412 Start – loads addresses 0 to 400 with the address of an interrupt routine that just does RTIs allowing looping in that part of the test where interrupt vector problems are occurring. Normal testing will then begin.

2. 1334 Start – load addresses 0 to 400 with trap catcher code. Any interrupt to this region will halt. Normal testing will then begin.

As soon as testing starts, the operator can change the switch register only by a 'BREAK' and manually loading location 176 (SWREG) with the desired contents; then doing a 'P' to proceed.

The user can select a specific test to be executed by setting bit 8 in SWREG and the test number (in octal) in bits <7:0>.

NOTES: All tests previous to the selected one are executed without iterations except test 22 which cannot be looped.

This diagnostic follows the standard procedure for running under APT;XXDP+ monitors as described in their respective procedures manual and SYSMAC package.

4.12 Operational Switch Settings

The software switch register (location 176) is used for all operational switch settings as follows.

1. Type Control G <^G>. This allows the TTY to enter data into location 176 at selected points within the program.

2. The machine then types: 'SWR=XXXXXX NEW=' (XXXXXX is the octal contents of the software switch register).

3. After the 'NEW=' has been typed the operator can do one of the following at the TTY:

   a. Type a number to be loaded into location 176 followed by a <CR>. (Only octal numbers from 0 to 7 are accepted.) Leading zeros need not be typed, and if more than six digits are typed only the last six are used. If a <CR> is the first key pressed the software switch register contents does not change.

   b. If a control U <^U> is pressed, the program sends you back to step 3.

   c. If the input character is not one of the characters mentioned above, a question mark (?) is typed, followed by a carriage return and a line feed sequence. Then proceed from step 2 (erasing all previous input).

4. The diagnostic continues running <CR>.

NOTE: Because of the frequent bus resets in the program, multiple control Gs may be required. If necessary, 'BREAK' into the program and load location 176 (SWREG) by 'ODT' to the desired contents. Do a 'P' to proceed.

Software Switch Register Options (SWREG)

Bit 15 set	=	100000	=	Halt on error
14 set	=	40000	=	Loop on test (to be used only while testing in progress)
13 set	=	20000	=	Inhibit error typeouts
12 set	=	10000	=	Enable performance reports
11 set	=	4000	=	Inhibit iterations
10 set	=	2000	=	Bell on error
9 set	=	1000	=	Loop on error
8 set	=	400	=	Loop on test in SWR<7:0>
7:0	=			Number of test to loop on (used with bit 8) (all tests previous to the selected test are executed first with 1 iteration only)

NOTE: If bit 14, 9, or 8 is selected the LEDs on the MXV11-B module may give false test number indications. If a test has a UNIBUS reset command, the LEDs will light fully every pass through the reset instruction. Thus, test 7 appears as test 17 (all LEDs on).

PROGRAMMING SUMMARY A

A.1 INTRODUCTION

This appendix summarizes programming the MXV11-B regarding the page control register, diagnostic display register, line time clock register, and the serial line unit (SLU) registers. Figure A-1 shows the bit assignments of the MXV11-B registers. For additional details, refer to Chapter 2.

A.2 PAGE CONTROL REGISTER

The PCR format and bit assignments for the page control register (PCR) are shown in Figure A-2. Bits 0–4 point to one of 32 256-word blocks in ROM (8K word space). The block pointed to is read through bootstrap address 773000_8. Bits 8–12 point to 1 of 32 256-word blocks in ROM. The block pointed to is read through bootstrap address 765000_8.

The PCR resides at location 777520 in the I/O page, and is enabled when the MXV11-B has its console and boot functions enabled.

A.3 DIAGNOSTIC DISPLAY REGISTER

The diagnostic display register (DDR) is a four-bit write-only register. Four LEDs correspond to the four register bits shown in Figure A-3. The DDR resides at location 777524 in the I/O page, and is enabled when the MXV11-B has its console and boot function enabled. At power up, the DDR is cleared and all LEDs are lit. The LEDs turn off when a logical one is written into that bit.

A.4 LINE TIME CLOCK REGISTER

The line time clock register (address 777546) is a one-bit register (bit 06). When bit 06 is set, the clamp is removed from BEVENT enabling the line time clock (LTC). The LTC resides at location 777526 in the I/O page and is enabled when the MXV11-B has its console and boot functions enabled.

A.5 SERIAL LINE UNIT PROGRAMMING

SLU 0 may be assigned to any one of eight starting locations in the I/O address space range from 776500 to 776570. SLU 1 is automatically assigned by the MXV11-B module to the next higher starting address over SLU 0. The I/O address assignment for SLU 1 is from 776510 to 776600.

When SLU 1 is assigned the console port, it assumes address 777560. Default addresses are 776500 for SLU 0 and console port for SLU 1.

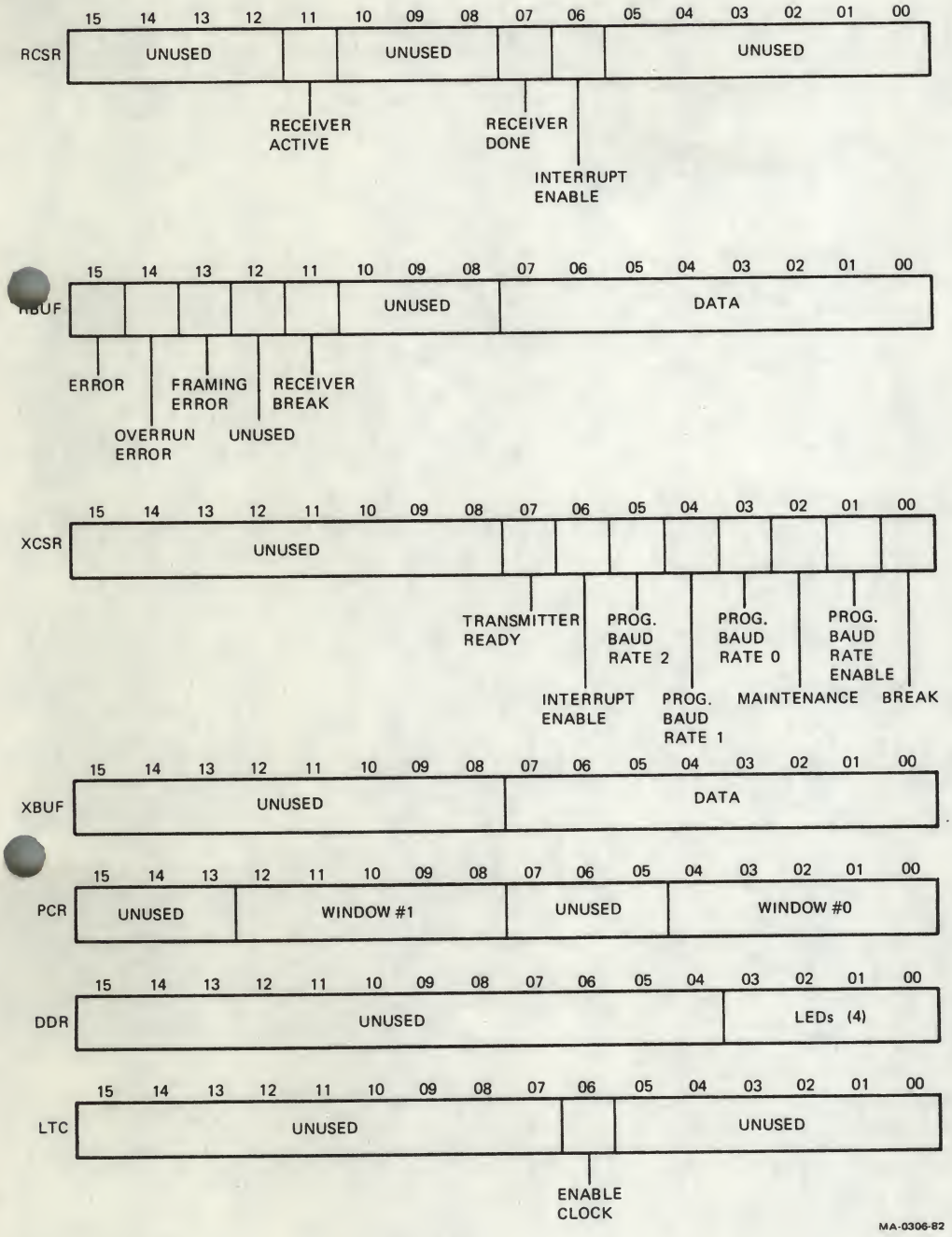


Figure A-1 MXV11-B Register Bit Formats

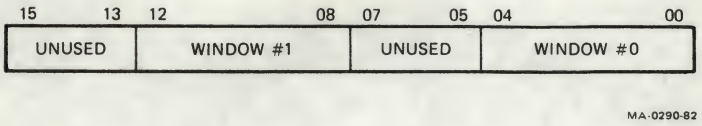


Figure A-2 Page Control Register

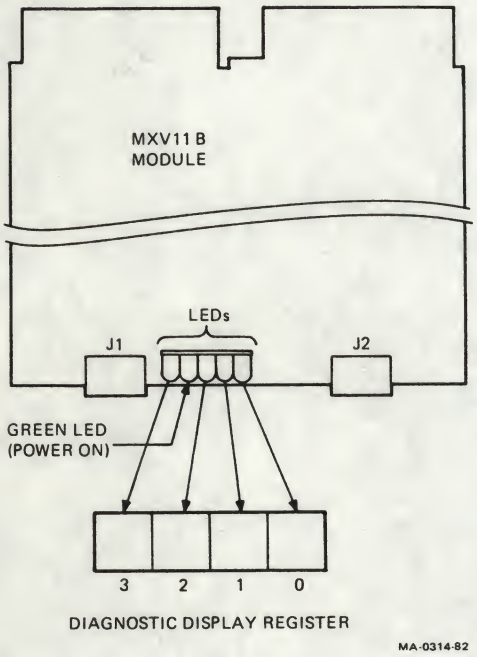


Figure A-3 MXV11-B Diagnostic Register (LEDs)

A.5.1 Interrupt Vector Selection

Vector address selection covers the vector address space from 010 through 376.

NOTE: Be careful – some addresses are reserved.

Bits 3–7 of the vector address can be programmed (via wire-wrap) to select independent vector addresses for each of the SLUs. Bits 0, 1, and 8 are always 0 for the MXV11-B.

A.5.2 SLU Registers

The MXV11-B has four registers for each of the two SLUs. The registers for both SLUs are addressed via address bits 2, 1, and 0, as shown below.

Receiver control and status register	– base address +0
Receiver data buffer	– base address $+2_8$
Transmitter control and status register	– base address $+4_8$
Transmitter data buffer	– base address $+6_8$

The bit assignments of each of the registers is described in Tables A-1 through A-4.

A.6 DIRECT MODE BOOT ADDRESSING

Users programming their own boot ROMs in direct addressing mode should realize that the addresses are not normalized. There are 2 256-word blocks that can be accessed in the I/O page on the MXV11-B. One 256-word block resides at 773000–773776 and the other at 765000–765776. The actual PROM location being addressed depends on the bus address and the PROM size used. Bus addresses increment by two while PROM addresses increment by one. For example, with a bus address of 765002 the corresponding PROM address is 2401 for a 2K by 8 PROM; 2401 for a 4K by 8 PROM, and 12401 for an 8K by 8 PROM (see chart below).

Bus Address	**Actual PROM Address**		
(256 words)	**2K × 8**	**4K × 8**	**8K × 8**
765000–765776	2400–2777	2400–2777	12400–12477
773000–773776	1400–1777	5400–5777	15400–15777

Bit 0 of bus address is a byte pointer (bus addresses increment by 2)
Bits 1–11 of bus address addresses 2K × 8 PROMs
Bits 1–12 of bus address addresses 4K × 8 PROMs
Bits 1–13 of bus address addresses 8K × 8 PROMs

Table A-1 Receiver Status Register Bit Assignments (RCSR)

Bit		Description
15–12		Unused
11	RA Receiver active read only	Receiver is active (logic 1)
10–8		Unused
7	RD Receiver done read only	SLU has received a character (logic 1)
6	IE Interrupt enable read/write	Enables receiver interrupts (logic 1)
5–0		Unused

Table A-2 Receiver Data Buffer Bit Assignments (RBUF)

Bit		Description
15	ER Error read only	Bit 13 and/or bit 14 is a 1 (logic 1)
14	OE Overrun error read only	Word in RBUF not read when another word was received in RBUF. (logic 1)
13	FE Framing error read only	Start bit but no stop bit (logic 1)
12		Unused
11	RB Receiver break read only	SI signal goes from mark to a space and stays for 11 bit times. (logic 1)
10–8		Unused
7–0	Data read only	Holds most recent byte (logic 1)

Table A-3 Transmitter Status Register Bit Assignments (XCSR)

Bit		Description
15–8		Unused
7	TR Transmitter ready read only	SLU ready to accept character (logic 1)
6	IE Interrupt enable read/write	Enables transmitter interrupt (logic 1)
5–3	BR2–BR0 Programmable baud rate select read/write	Determines software programmable baud rate (when PBR = logic 1).
2	MAINT Maintenance read/write	Connects serial output to serial input. External serial input disconnected (logic 1)
1	PBR Programmable baud rate enable/inhibit PBR read when programmable baud rates enabled (SOFT to GND jumper); else read/write	Selects hardware or software baud rates (logic 1 for software; logic 0 for hardware).
0	BK Break read/write	Causes serial output to go to Space condition (logic 1).

Table A-4 Transmitter Data Buffer Bit Assignments (XBUF)

Bit		Description
15–8		Unused
7–0	XMIT DATA BUFFER read/write	Holds a copy of the most recent byte written into it. (logic 1)

MXV11-B MULTI-FUNCTION OPTION MODULE
USER GUIDE

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